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SGM2014M	UHF Amp, Mixer, Osc	1.5dB @900MHz	18dB	17mS	0.9pF	Yes	Minimold	4
3SK165	UHF Amp, Mixer,Osc	1.2dB @800MHz	20dB	22mS	0.5pF	–	Minimold	4
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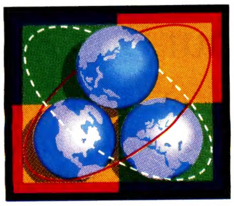

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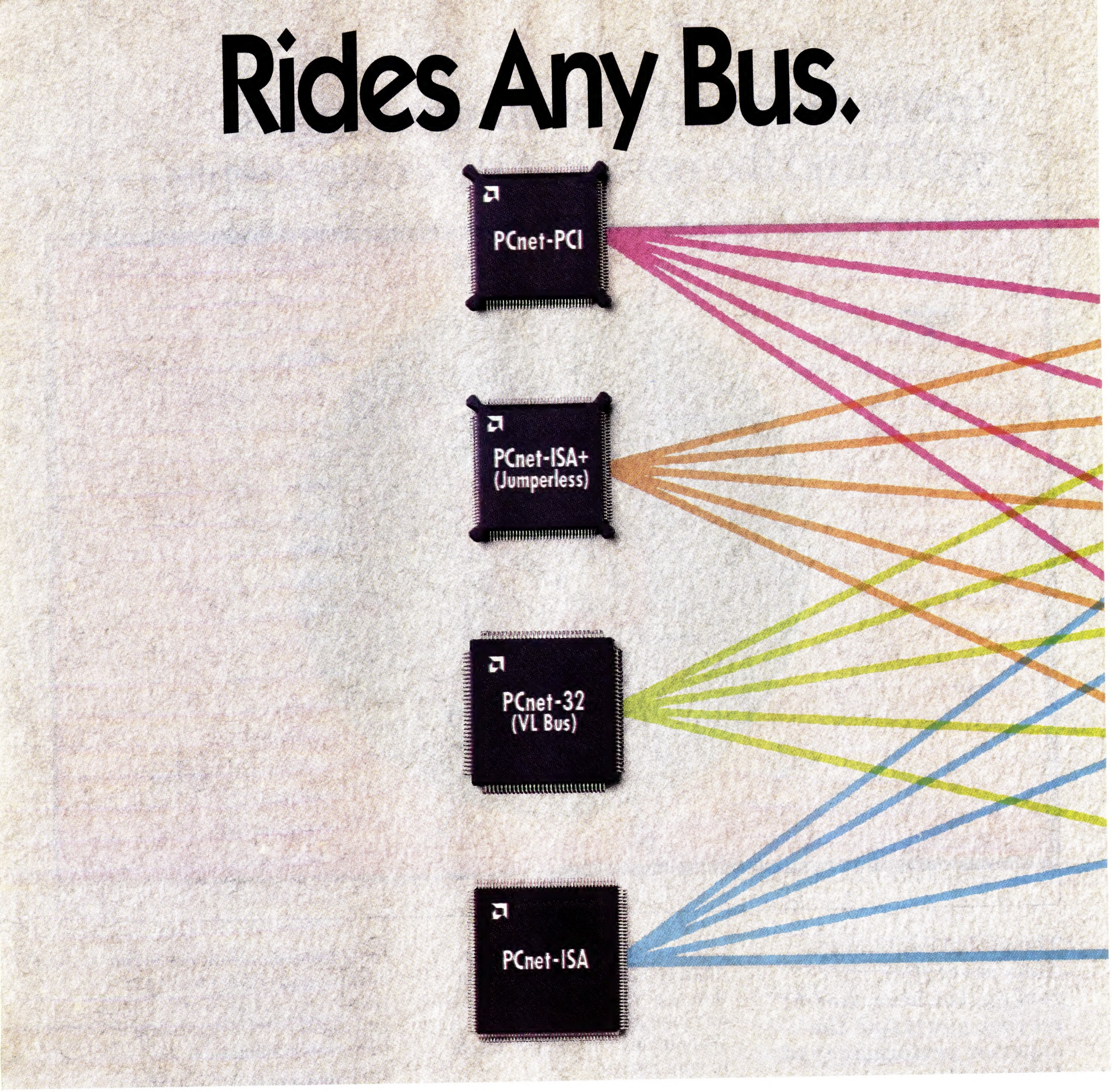

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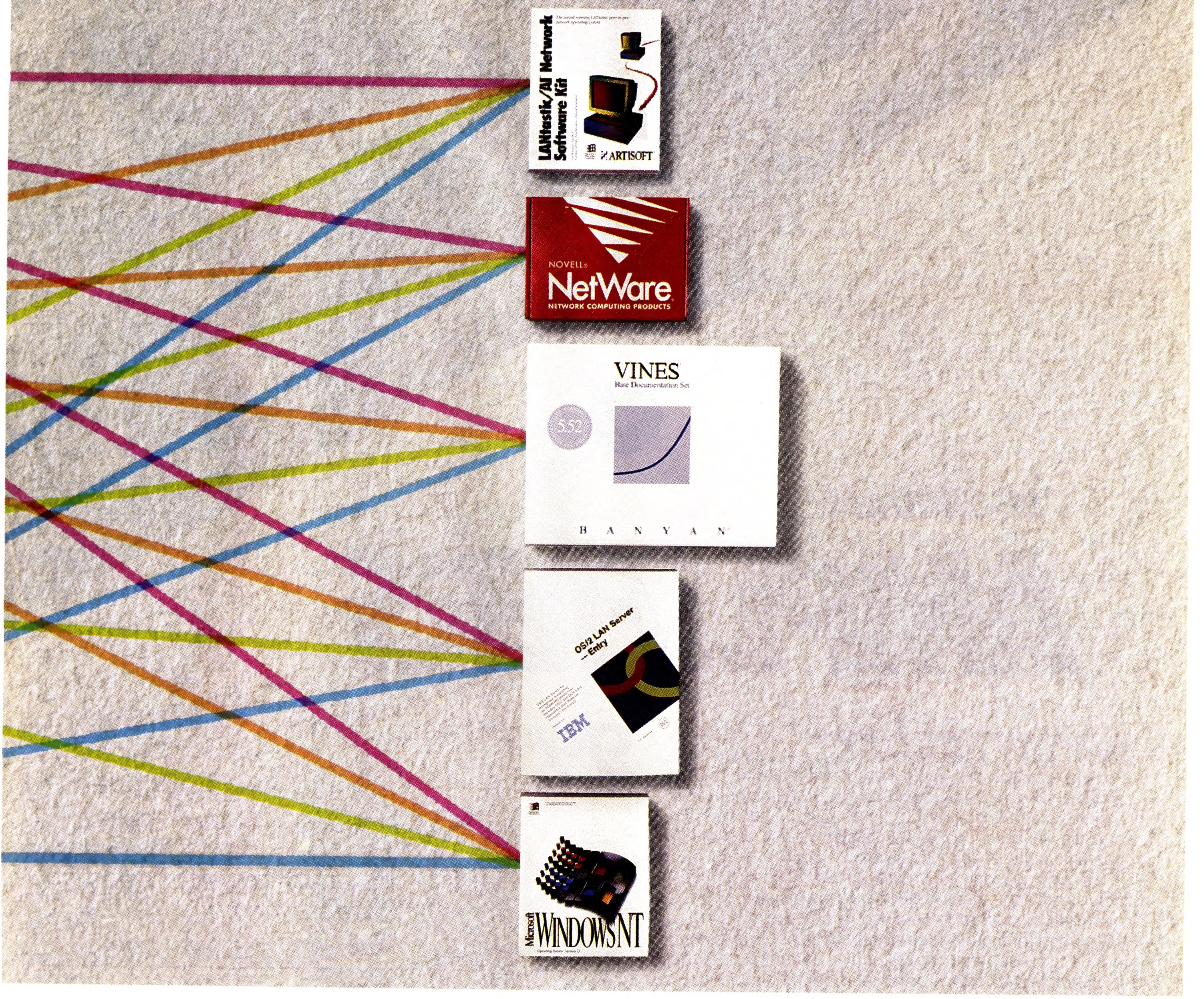

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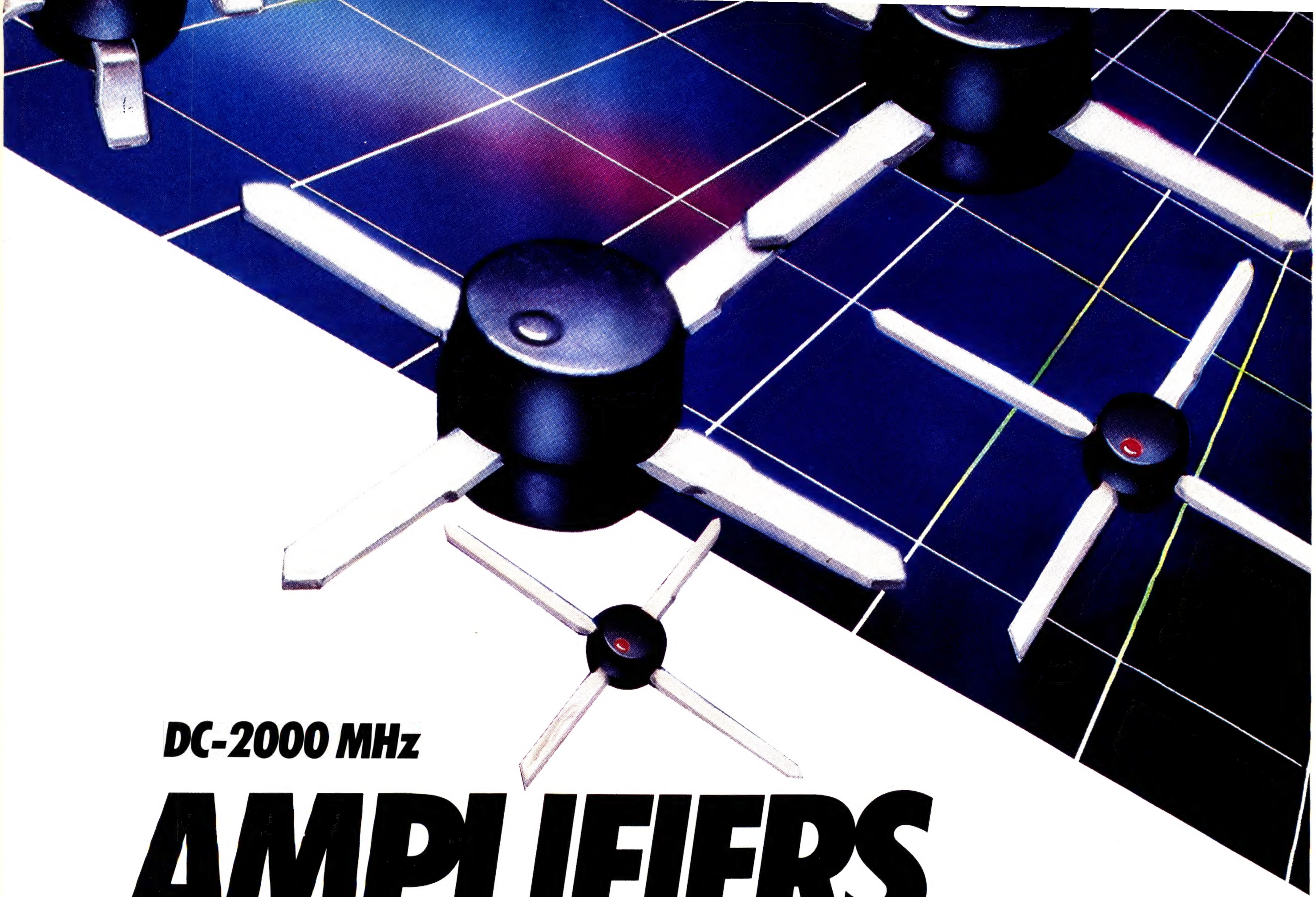

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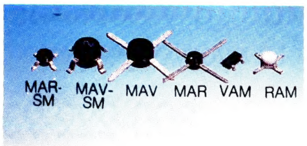

Models above shown actual size

from **99¢** Unit price $ (25 qty)

PLASTIC SURFACE-MOUNT			++VAM-3 1.45		+VAM-6 1.29	++VAM-7 1.75		
add suffix SM to model no. (ex. MAR-ISM)	MAR-1 1.04	MAR-2 1.40	MAR-3 1.50	MAR-4 1.60	MAR-6 1.34	MAR-7 1.80	MAR-8 1.75	
	MAV-1 1.15	+MAV-2 1.45	+MAV-3 1.55	MAV-4 1.65				MAV-11 2.15
CERAMIC SURFACE-MOUNT	RAM-1 4.95	RAM-2 4.95	RAM-3 4.95	RAM-4 4.95	RAM-6 4.95	RAM-7 4.95	RAM-8 4.95	
PLASTIC FLAT-PACK	MAV-1 1.10	+MAV-2 1.40	+MAV-3 1.50	+MAV-4 1.60				MAV-11 2.10
	MAR-1 0.99	MAR-2 1.35	MAR-3 1.45	MAR-4 1.55	MAR-6 1.29	MAR-7 1.75	MAR-8 1.70	
Freq.MHz,DC to	1000	2000	2000	1000	2000	2000	1000	1000
Gain, dB at 100MHz	18.5	12.5	12.5	8.3	20	13.5	32.5	12.7
Output Pwr. +dBm	1.5	4.5	10.0	12.5	2.0	5.5	12.5	17.5
NF, dB	5.5	6.5	6.0	6.5	3.0	5.0	3.3	3.6

Notes: + Frequency range DC-1500MHz ++ Gain 1/2 dB less than shown

designer's amplifier kits
DAK-2: 5 of each MAR-model (35 pcs), only $59.95
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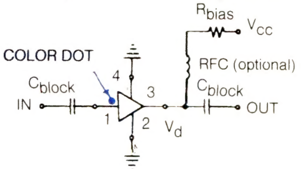
designer's chip capacitor kit
KCAP-1: 50 of 17 values, 10pf to 0.1μf (850 pc), $99.95

chip coupling capacitors at .12¢ each (50 min.)

Size (mils)	Value
80 x 50	10, 22, 47, 68, 100, 220, 470, 680 pf
80 x 50	1000, 2200, 4700, 6800, 10,000 pf
120 x 60	.022, .047, .068, .1μf

Typical Circuit Arrangement



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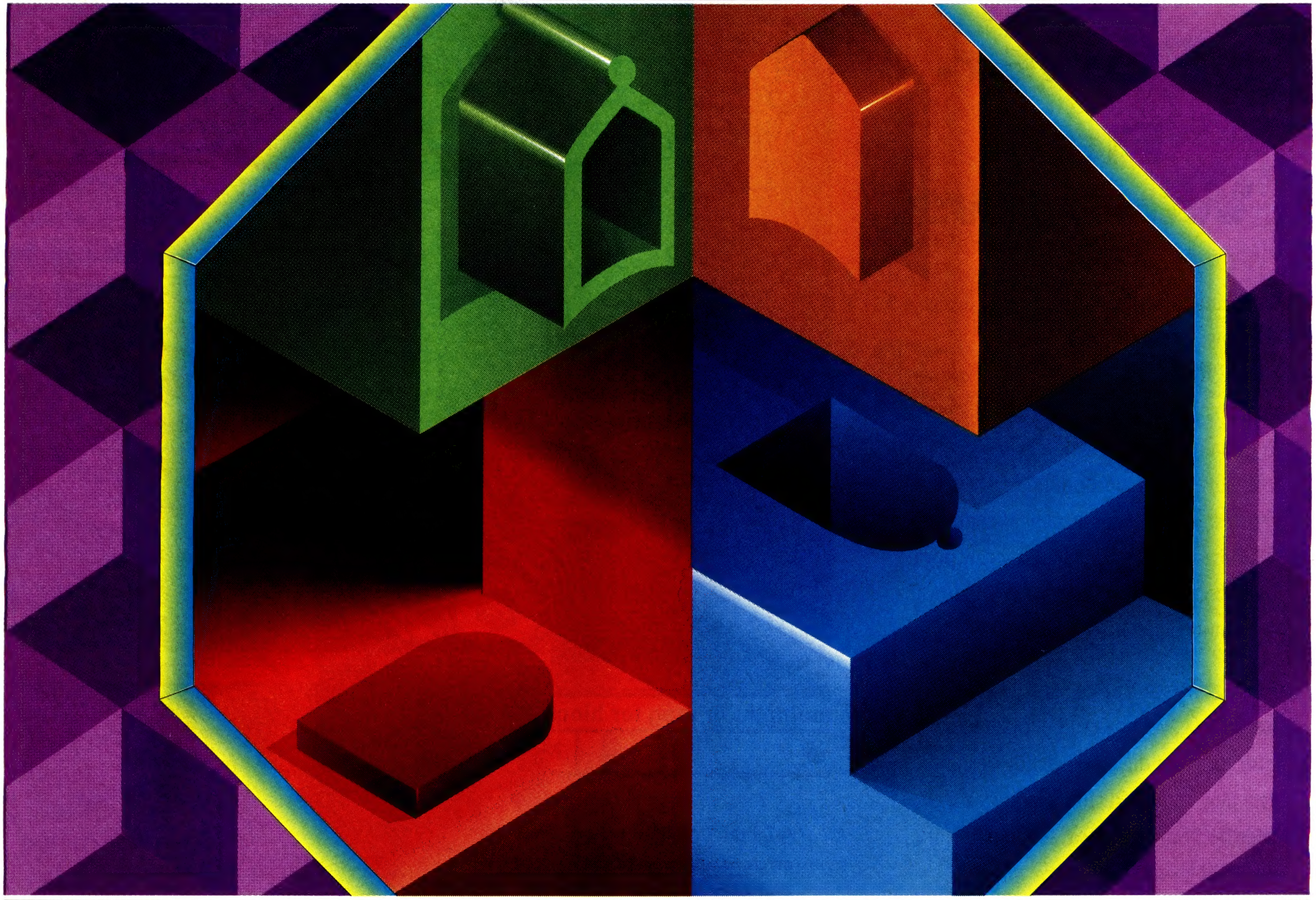
MARCH 21, 1994 VOL. 42, NO. 6

ELECTRONIC DESIGN



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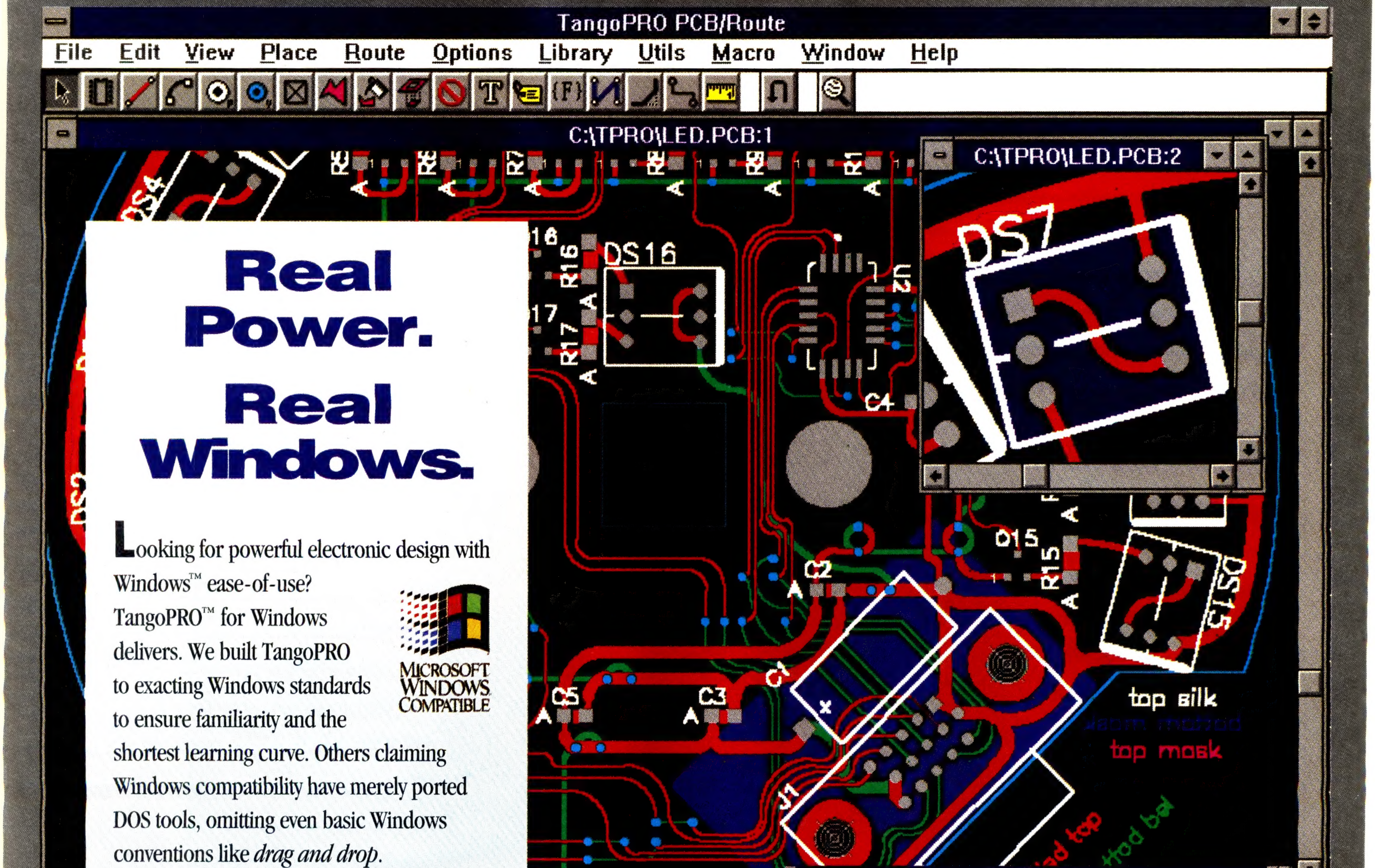

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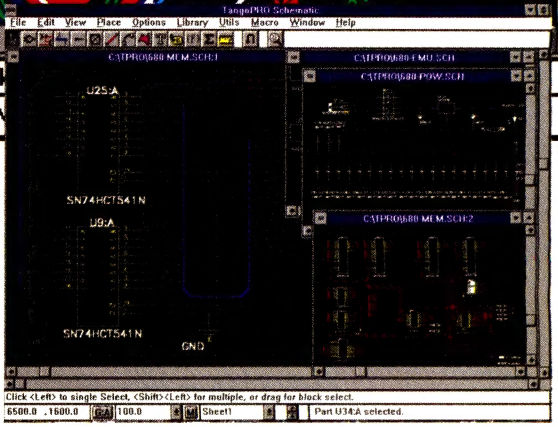

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ELECTRONIC DESIGN

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- Designing mixed 5-V/3-V systems
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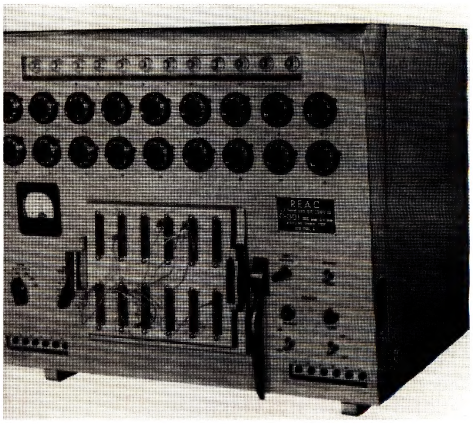
ELECTRONIC DESIGN 40 YEARS AGO

Compact computer design

Functional versatility, small size, attractive appearance and ease of maintenance were the design goals set when the new Reeves Desk-top Computer was planned. Norman Zatsky, Chief Mechanical Engineer of the manufacturer, Reeves Instrument Corp., 215 East 91st St., New York 28, N.Y., is responsible for the neat mechanical design of the computer. Only 20" x 25" x 20" in size, the 150-lb unit does the same job as conventional equipment that occupies a seven-foot cabinet two feet wide. Featuring exceptional stability, the computers can solve differential equations or simulate physical systems with a component accuracy of 0.1%. For maximum use and flexibility, problems can be set up on one removable patchboard while the computer is solving another problem, using a second board.



Made in two models, the computers are entirely self-contained. Each model contains 12 individually chopper-stabilized computing amplifiers, which have extremely low noise, drift of less than 0.25mv per day, d-c gains of more than 15,000,000, flat frequency response, and full load output over a range from –100v to +100v. The amplifiers are made with printed-and-etched wiring on ethoxyline-impregnated glass fiber sheets mounted on metal frames. All resistors and capacitors are soldered for reliability and ease of maintenance. Thyrite varistors protect the choppers. For greater amplifier output, the specified 12AV7 output tube in more than half the amplifiers can be replaced with a 5687 by using a tube adapter. If still greater power output is needed, an amplifier of different design using a 5687 tube in the output stage can be supplied. Space-saving was accomplished in the regulated power supply by the use of junction germanium rectifiers. The REAC Series 300 Desk-top Computers will be demonstrated at Booths 341-347 at the Radio Engineering Show. *(Electronic Design, March 1954, p. 16.)*

It's interesting that nowhere in this item is the computer identified as an analog computer. The idea of a desktop digital computer apparently was so far from reality that the editors saw no need to make the distinction.—SS

Books: Theory and Design of Electron Beams, J.R. Pierce, second edition, 222 pages. D. Van Nostrand Company, Inc., $4.50.

The second edition of this excellent work on electron beams includes added material on focusing in the presence of space charge as well as a whole new chapter on focusing by means of periodic fields. The book presents the minimum amount of theoretical material necessary for a good understanding of electron flow and electron focusing in devices other than electron microscopes and image tubes. The first seven chapters cover basic material on electron flow in terms of fundamental laws and principles. The remaining five chapters deal with the effect of thermal velocities, space charge in electron beams, electron guns, periodic focusing fields, and a few cautions that should be observed when designing electron beam devices. This book definitely deserves a place on every tube designer's reference shelf, and circuit designers will find much material of interest from the point of view of gaining clearer insight into the inner working of electron beam devices. *(Electronic Design, March 1954, p. 72.)*

The control of electron beams is no longer commonly taught in EE curricula, but it was a challenging course, involving extensive calculations of the effects of acceleration and focus voltages on a beam of mutually repelling particles. This book's author, John R. Pierce of Bell Laboratories, was an early visionary in satellite communications systems and a pioneer in the design of traveling-wave tubes.—SS

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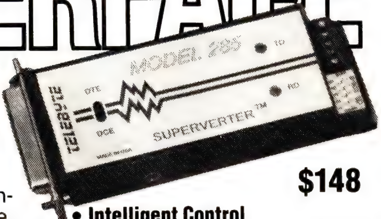
INTERFACE



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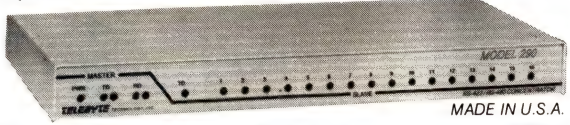

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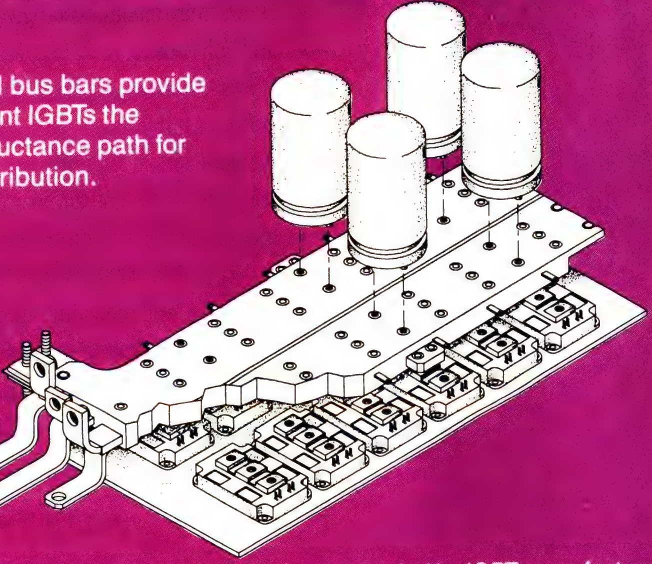

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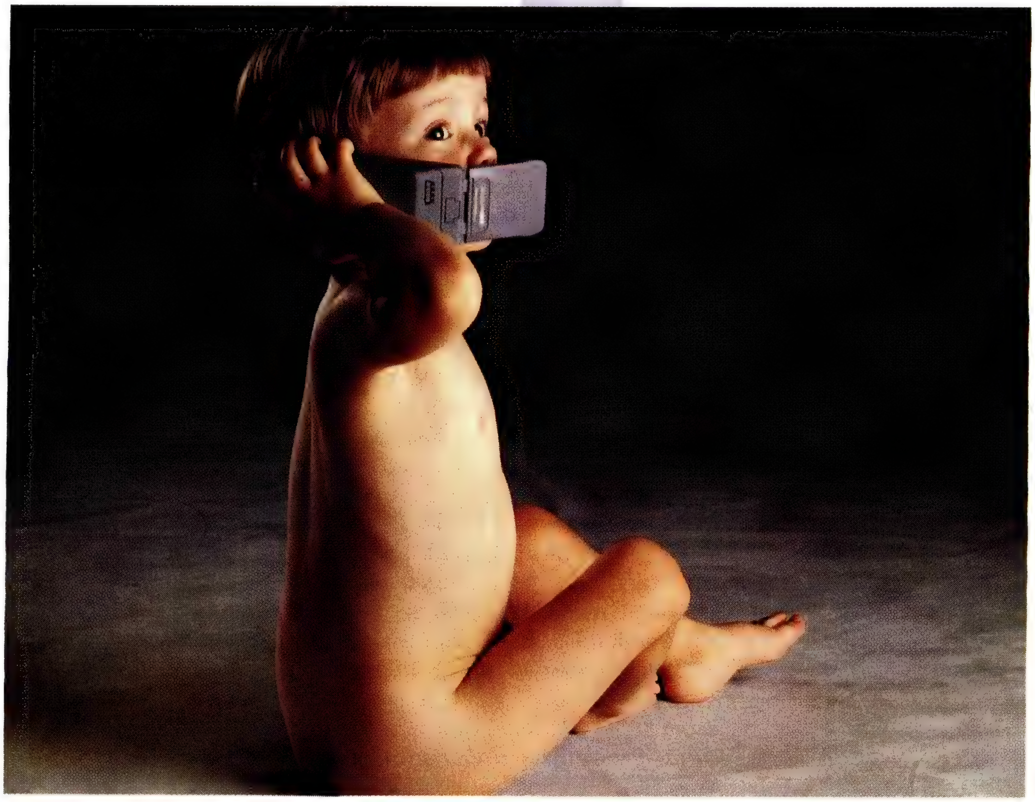

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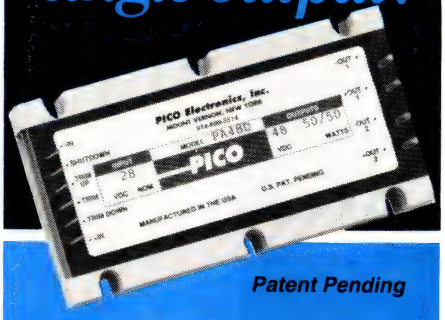

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UPCOMING MEETINGS

MARCH

1994 IEEE National Radar Conference, Mar. 29-31. Holiday Inn Crowne Plaza, Ravinia, Atlanta, GA. Contact Dr. Robert N. Trebits, Georgia Tech Research Inst., 7220 Richardson Rd., Smyrna, GA 30080; (404) 528-7769; fax (404) 528-7883.

SOUTHCON '94, Mar. 29-31. Orange County Convention/Civic Center, Orlando, FL. Contact Ms. JoAnn Lindberg, ECM, 8110 Airport Blvd., Los Angeles, CA 90045; (800) 877-2668; fax (310) 641-5117.

APRIL

SOUTHEASTCON '94, Apr. 10-13. Hyatt Regency Hotel, Miami, FL. Contact Dr. Osama A. Mohammed, Dept. of Elec. Eng., Florida Int'l University, University Park Campus, Miami, FL 33199; (305) 348-3040/3708; fax (305) 348-3707.

1994 IEEE International Reliability Physics Symposium, Apr. 11-14. Fairmont Hotel, San Jose, CA. Contact Ajit Goel, Oneida Research Services, 540 Weddell Dr., Ste. 7, Sunnyvale, CA 94089; (408) 734-2982; fax (408) 734-2984.

Embedded Systems Conference East, Apr. 19-21. Hynes Convention Ctr., Boston MA. Contact John Huber, Embedded Systems Conference, 600 Harrison St., San Francisco, CA 94107; (415) 905-2354; fax (415) 905-2220.

1994 IEEE International Conference on Acoustics, Speech & Signal Processing (ICASSP '94), Apr. 19-22. Adelaide Convention Ctr., Adelaide, S. Australia. Contact Phil Plevin, Plevin & Associates Pty. Ltd., P.O. Box 54, Burnside 5066, S. Australia; (61) 8-379-8222; fax (61) 8-379-8177.

1994 IEEE 44th Electronic Components and Technology Conference (ECTC '94), Apr. 30-May 5. Washington Hilton Hotel, Washington D.C. Contact James Bruorton, Kemet Electronics, P.O. Box 5928, Greenville, SC 29606; (803) 963-6621; fax (803) 963-6521.

MAY

1994 IEEE Custom Integrated Circuits Conference (CICC '94), May 1-4. Town & Country Hotel, San Diego, CA. Contact Melissa Widerkehr, Widerkehr and Assoc., 1545 18th St. NW, Washington D.C. 20036; (202) 986-2166; fax (202) 986-1139.

VHDL International Users' Forum (VIUF), May 1-4. Co-located with the CFI 1994 Conference, Claremont Resort & Spa, Oakland, CA. Contact Ronald Waxman, University of Virginia, Dept. of EE, Thornton Hall, Charlottesville, VA 22903-2442; (804) 924-6986; fax (804) 924-8818; E-mail: Ronw@virginia.edu.

ICC/Supercomm '94 - 1994 International Conference on Communications, May 1-5. Ernest N. Morial Convention Center, New Orleans, LA. Contact Eddie Sawaya, So. Central Bell Telephone, 365 Canal St., Room 710, New Orleans, LA 70140; (504) 528-2673; fax (504) 528-7170.

Networld + Interop 94, May 2-6. Las Vegas, NV. Contact Nancy Garafano, Ziff-Davis Exposition and Conference Co., 303 Vintage Park Dr., Foster City, CA 94404-1138; (415) 578-6900; fax (415) 525-0194.

1994 Electronic CAD Interoperability and Integration Conference (EII'94), May 4-6. Claremont Hotel, Oakland, CA. Contact Don Cottrell, Program Chair, CAD Framework Initiative Inc., 4030 W. Braker Ln., Suite 550, Austin, TX 78759; (512) 338-3379; E-mail: Contrell@cfi.org.

1994 IEEE International Conference on Robotics and Automation, May 8-13. San Diego Princess Resort, San Diego, CA. Contact Harry Hayman, Box 3216, Silver Spring, MD 20918; (301) 236-5621; fax (301) 236-5621.

1994 Conference on Lasers & Electro-Optics/The International Electronics Conference (CLEO/IQEC), May 8-13. Anaheim Convention Center, Anaheim, CA. Contact IEEE/LEOS, 445 Hoes Ln., P.O. Box 1331, Piscataway, NJ 08855-1331; (908) 562-3893; fax (908) 562-1571.

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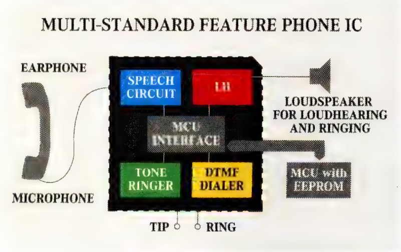

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READERS COME FIRST

Sometimes it pays to step back and check to see exactly what service you're providing. It's not always obvious. *Electronic Design* is (and always has been) an information provider. More specifically, our editors collect, select, compare, and take pains to understand the avalanche of raw information that passes over our desks, through our modems, and into our ears every day.

When we finish that formidable task, we recast the alphabet soup of technology-specific jargon into something EEs who work in other disciplines can readily understand. Only after that do we publish it.

Every successful venture knows its niche. *Electronic Design* has always excelled at the "understanding" part of the formula I postulated a couple of paragraphs ago. We strive to understand not just what a product or technology does, but also to understand what impact it will have on engineers. That perspective is why we consistently do so well in readership surveys. We write with the reader in mind, something that's easier said than done.

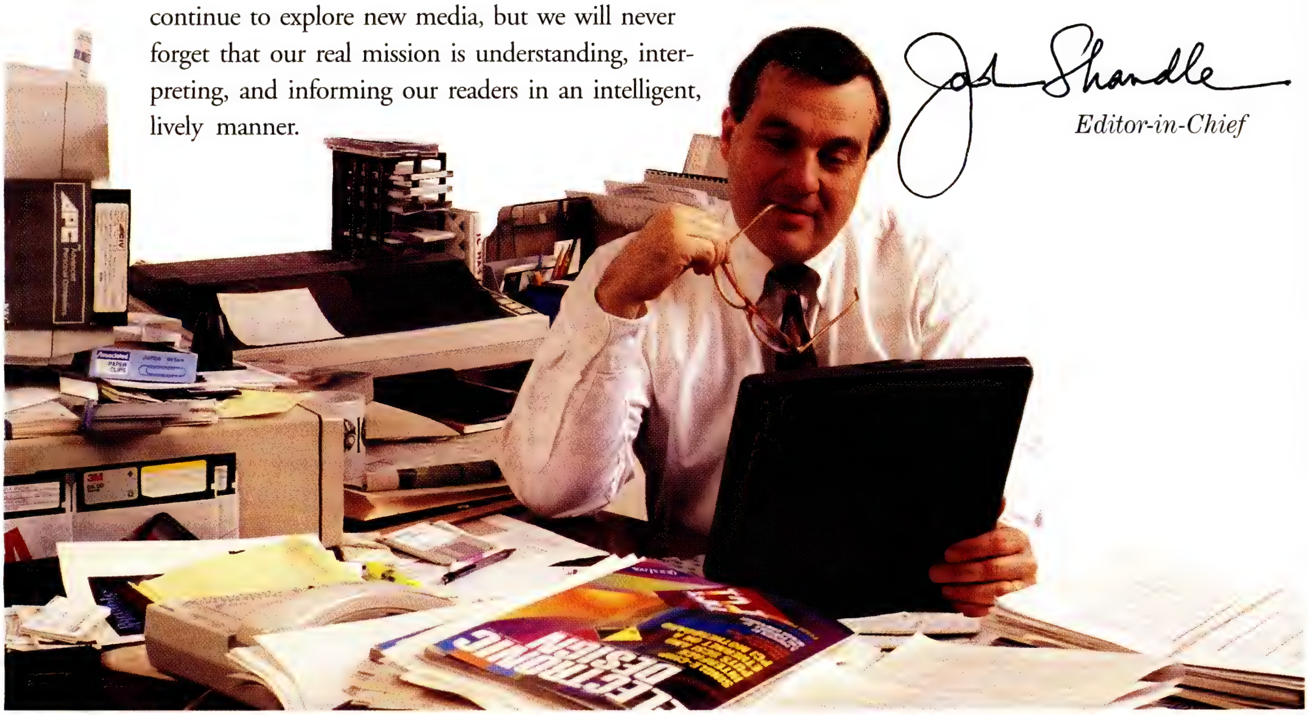
As the new editor-in-chief of *Electronic Design,* my job will be to build on that tradition. Although we're moving into new media—Five Years of Electronic Design on CD-ROM and the Portable By Design Conference are just two examples—these initiatives will always be reader-driven.

Because *Electronic Design* is in the information business (not solely the magazine publishing business), an important part of our charter is to mobilize new media as soon as it matures enough to become an efficient vehicle for a new productivity tool. *Electronic Design,* the magazine, will always be the centerpiece of the suite of productivity tools that Editorial Director Steve Scrupski and I are putting together along with our staff. If anything, the magazine will grow stronger because it must serve as the fulcrum upon which the ancillary tools will be leveraged.

No less a pundit than Microsoft's Bill Gates often refers to paper as a very tough opponent for electronic media. Paper as an information distribution medium has, after all, been tuned to near perfection for several hundred years. You can't carry a CD-ROM in your hip pocket yet, and you can't read it without a drive. Paper is portable, familiar, and surprisingly durable.

But looking at media as competing technologies really misses the point. Over the coming years, we will continue to explore new media, but we will never forget that our real mission is understanding, interpreting, and informing our readers in an intelligent, lively manner.

Jack Shandle
Editor-in-Chief



NEW MEDIA, NEW STRUCTURE

Electronic Design magazine, since its founding in 1952, has had a compact with its readers to publish all of the technology, design, and product news needed for electronics design engineers to keep up-to-date and current with the state-of-the-art in electronics technology. However, the past few years has seen profound changes occur in publishing media. New electronic avenues for disseminating information continue to emerge, while the information needs of design engineers are forever shifting. Through all of these changes, the print medium still flourishes, and, I believe, will do so for years to come. But it no longer is the only means of delivering information to the world's design engineers.

Electronic media—CD-ROMs, facsimile, and computer-based communications—have taken hold, each offering a special set of facilities that are ideal for certain applications. *Electronic Design*, being an information resource, would be remiss if it did not grow along with these changes and fulfill its role as a leader in its own industry.

Therefore, Electronic Design is moving beyond the strict borders of print to offer new information vehicles to its readers. We have expanded our charter from just a single magazine to a multifaceted information resource—we now are calling ourselves the *Electronic Design Information Group*. The magazine itself will continue to be the centerpiece of the group, but our internal structure will change to accommodate this expanded vision of our future.

The first of these changes recently took place: I have moved to a new position within our organization, Editorial Director for the *Electronic Design Information Group*. Jack Shandle, *Electronic Design's* Advanced Technology Editor for the past two years, is now Editor-in-Chief of *Electronic Design*. Jack is well-qualified for the job: He is an EE who also holds a degree in journalism. As Editorial Director for this newly formed organization, I will research changing reader needs and emerging technology niches that might require new efforts beyond what can be achieved in the pages of *Electronic Design* magazine.

As Jack mentions in his column at the left, our latest efforts are a CD-ROM containing the last five years of *Electronic Design* and the recent Portable by Design conference. In our February 21 issue, we introduced the Engineering Software Supplement, which will appear four more times this year. In the future, there will be other such special information products to serve our primary customers—you, our readers.

Steve Scrupski

Editorial Director
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MORE ON THE RADIOTRON HANDBOOK...

I was fascinated to read your short article on the Radiotron Designers Handbook in the Nov. 11, 1993 issue.

I bet you didn't know that this book was actually written and edited in Australia by the engineers at Amalgamated Wireless Australasia Ltd., now AWA Ltd.

The original was titled Radio Designers Handbook and was published in a number of languages including Japanese. RCA published it in the USA and changed Radio to Radiotron in the title.

JIM SPENCE
TECHNICAL OPERATIONS MANAGER
AWA LTD.
LANE COVE, NSW, AUSTRALIA

...AND MORE AGAIN ON THE GIBSON GIRL

Your editorial in the December 2, 1993 issue caught my eye at this late date in my capacity as secretary and editor of the publications of the Society of Wireless Pioneers. I managed to locate the Sept. 2, 1993 issue referred to in your "40 Years Ago" item, which raised the subject to awareness level.

The subject was the 56-lb. "Gibson Girl" automatic emergency radio that was manufactured just before the USA was hit at Pearl Harbor. I was working on that production line at Bendix Corp., in N. Hollywood, Calif., until I was taken off the line to become secretary to one of production managers because I could type!

My memory of the "Gibson Girl" transmitter is quite strong, as I was privy to her innards in a way shared by very few of those who used her over the years of World War II. I tested many of her clones between my thighs at the end of the line, in the shielded room where no stray SOS signals would leak out to bring ships up to our front or back door! And then, to top the experience with frosting, as I was returning to the US from my naval World War II assignment in Australia, via FAT (first available transportation), which happened to be on a "Flying Fortress," we hit a typhoon and crew and passenger (yours truly) just missed ditching in the ocean between Biak-Pellieu and Manila—the Gibson Girl and a life raft were readied for the anticipated plunge into the drink. I'm sitting here at this keyboard so obviously we made it okay; but my memories are quite vivid of that orange-colored Gibson Girl!

In my capacity as editor of the Society of Wireless Pioneers *Sparks Journal*, I would like to collect additional information about experiences with the Gibson Girl. The primary purpose of the Society is to document and preserve for posterity the activities and exploits of the men and women who were, first of all, spark-gap wireless-telegraph operators at ship and shore stations, and as the years and the technology progress, each phase of wireless and its operators and technicians. We have, for instance, just recently documented the closing of watch-standing on 500-Hz SOS calling-frequency by the Coast Guard.

I'll pursue any lead that becomes available to round-out the story that we have yet to cover. My thanks to you for bringing it to my attention! It would have been a base oversight to have neglected the Gibson Girl in our publications.

Thank you for your interest, and for any help you can offer us toward documenting the Gibson Girl story. By the way, we have been granted a special historical shelf in the State Library of California for all of our publications to date and future. It will be open to the public some time this year.

WALDO T. BOYD, K6DZY
P.O. BOX 86
THE WORLD WIRELESS BEACON
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Editor's note: We're sending Mr. Boyd copies of the letters we have received about the Gibson Girl receiver, and we encourage readers to contact him if they have additional historical information.

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Isolation (dB)	42	31	20	50	40	28
1dB Comp. (dBm)	18	20	22.5	20	20	24
RF Input (max dBm)	——	20	——	22	22	26
VSWR "on"	1.25	1.35	1.5	1.4	1.4	1.4
Video Bkthru (mV,p/p)	30	30	30	30	30	30
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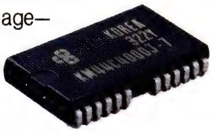
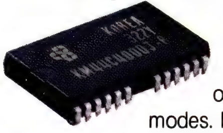


Samsung's 16M DRAMs have been optimally designed in x1/x4 and x8/x16 chip sets with fast access times of 50/60/70ns. A new extended data output(EDO)mode enhances access times over chips that use conventional fast page modes. Moreover, these chips are extremely energy efficient, drawing not 5volts, but a mere 3.3volts of power.



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4MX 4	Fast Page	KM44C(V) 4000A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4100A/AL/ASL/ALL	2048Cycle/32ms
	Static Column	KM44C(V) 4002A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4102A/AL/ASL/ALL	2048Cycle/32ms
	Quad-$\overline{\text{CAS}}$	KM44C(V) 4003A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4103A/AL/ASL/ALL	2048Cycle/32ms
	EDO (Hyper Page)	KM44C(V) 4004A/AL/ASL/ALL	4096Cycle/64ms
		KM44C(V) 4104A/AL/ASL/ALL	2048Cycle/32ms
2MX 8	Fast Page	KM48C(V) 2000A/AL/ASL/ALL	4096Cycle/64ms
		KM48C(V) 2100A/AL/ASL/ALL	2048Cycle/32ms
1MX16	Fast Page	KM416C(V) 1000/L/LL	4096Cycle/64ms
		KM416C 1200/L/LL	1024Cycle/16ms
1MX 4	Fast Page	KM44C(V) 1000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM44C(V) 1000C/CL/CSL/CLL	1024Cycle/16ms
	Quad-$\overline{\text{CAS}}$	KM44C(V) 1003C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM44C(V) 1004C/CL/CSL/CLL	1024Cycle/16ms
4MX 1	Fast Page	KM41C(V) 4000C/CL/CSL/CLL	1024Cycle/16ms
	Static Column	KM41C(V) 4000C/CL/CSL/CLL	1024Cycle/16ms
	EDO (Hyper Page)	KM41C(V) 4004C/CL/CSL/CLL	1024Cycle/16ms

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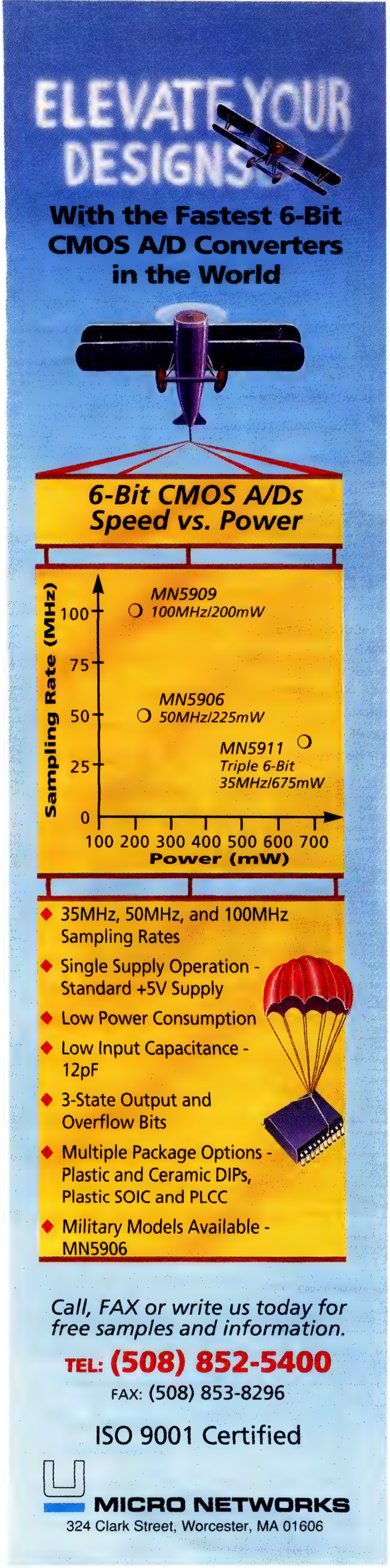

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KGD WILL SEED MCMS' FUTURE

If the future of microelectronics packaging lies in multichip modules (MCMs), then the future of MCMs lies in the availability of known-good die (KGD). Fears of KGD difficulties have kept many would-be MCM implementers from taking the plunge. Therefore, the KGD availability is key in making MCMs palatable to more systems houses. An important differentiator among the various KGD technologies in the industry is the means by which contact is made with the die for test and burn in.

Recently, the High-Value Electronics Division of MCC, Austin, Texas, completed the first phase of its KGD project by surveying the industry's KGD technologies. In a report delivered on March 9, MCC catalogued these approaches and provided guidelines for evaluating KGD technologies. The consortium, in its role as a technology developer for its member companies, is now in a good position to evaluate the existing approaches.

According to Larry Gilg, member of MCC's technical staff, 1994 will be a watershed year for KGD and for MCMs in general. "The technical challenges that have been surmounted in the last year or two were more formidable than people thought they would be," says Gilg.

DAVID MALINIAK
COMPONENTS & PACKAGING

MCC's report broke the approaches down into three separate means of making contact with the bare die: temporary contact, soft connections, and minimal packaging. Temporary contacts involve microminiature probes built into carriers intended to mimic standard packages. Soft connections mean non-standard (or rerouted) connections, such as wire bonds or C4 attachment, to a reusable standard package. Minimal packaging is a permanent carrier that provides the burn-in and test interface as well as a substrate vehicle.

As of now, the smart money seems to be on temporary-contact technologies. Although some soft-connection methods are already in production, they're somewhat labor-intensive, they don't invite automation, and they're I/O-limited. Despite success in using a soft-connection approach with its C4 bumped die, IBM is actively researching temporary-contact options, says Gilg.

Although minimal-package approaches appear to work, few, if any, of the semiconductor houses would want to be locked into any particular packaging technology. They want to use the die as they come off their fab lines, put them into carriers, and test and burn them in with their existing infrastructure.

From a cost standpoint, the jury is still out. From extensive cost modeling, MCC has determined that temporary contacts show promise provided that a given technology is capable of hundreds of reuses. That technology must also give users a sure-fire means of aligning the die within the carrier. Otherwise, the vision systems and automatic-placement equipment required to take up the slack would drive costs too high.

MCC found that in addition to the publicly acknowledged programs, there are others, mainly at large semiconductor houses, being kept under wraps. Gilg would only venture to say that while the semiconductor houses are making progress, they're not miles ahead of the programs surveyed. "Most are in alpha test, where they're actually doing some burn-in of die and evaluating the results. Those results have been mixed at best," says Gilg. The lone exception to the rule is IBM.

The second phase of MCC's KGD project moves from paper to hardware. After selecting the most promising technologies, MCC will put them to the test. The consortium has targeted a trial MCM implementation for late 1994 or early 1995. Once a technology has been settled on, qualification at the die supplier's site will begin. The final step will be insertion of KGD into the MCM. In the long run, MCC hopes that the KGD project will inspire confidence in a technology that holds so much promise yet provokes so much anxiety.

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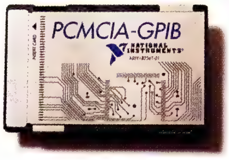

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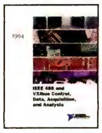

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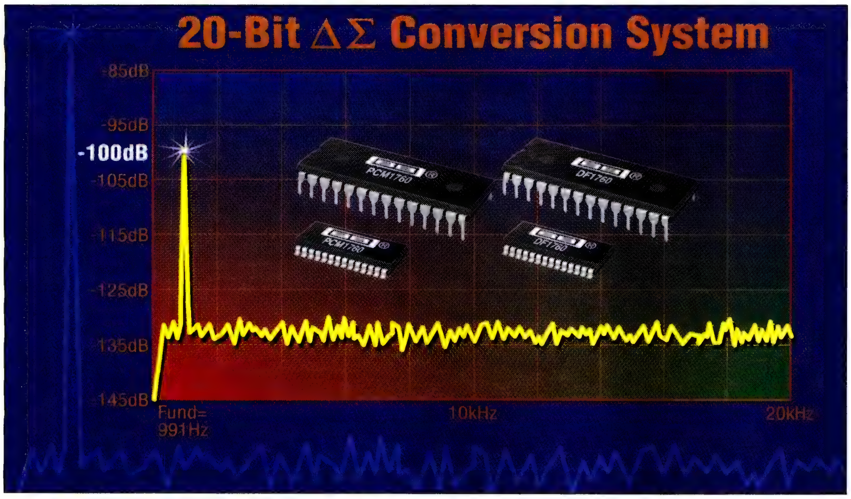
New Product Update



New 20-Bit Digital Audio ADC System

PCM1760 stereo delta-sigma modulator, together with its matched DF1760 digital filter, provide professional digital audio designers the best combination of analog-to-digital converter performance available for under $30! The system offers 20-bit resolution, wide 108dB dynamic range, very low –92dB THD+N, and clear 110dB SNR. PCM1760 and DF1760 are available in 28-pin DIP and SOIC. PCM1760 operates from ±5V supplies, DF1760 from a single 5V supply.

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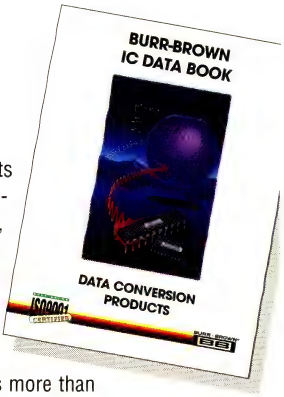
New Data Conversion Products IC Data Book



The Data Conversion Products IC Data Book contains complete product descriptions, specifications, applications tips, and ordering information for a broad line of high performance, high quality data conversion products. With over 950 pages, it offers more than 25 new high performance data conversion solutions. New products profiled include: A/D and D/A converters, data acquisition components, sample/hold amplifiers, V/F converters, multiplexers, and demonstration boards. The Data Conversion Products Data Book is **FREE** from any Burr-Brown sales office or representative.

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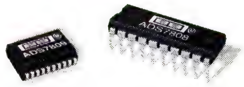
New



12- and 16-Bit Serial Out, 100kHz Sampling A/Ds

ADS7808 and ADS7809 are low cost, general purpose, serial output, CMOS sampling A/Ds. Both deliver 100kHz sampling rates with very low 100mW power dissipation using a single +5V supply. Ideal for many low power, portable applications requiring high sampling rates with superior accuracy and spectral purity, they're perfect for spectrum analyzers, portable oscilloscopes and vibration analyzers, medical electronics, and process control applications—where their serial output simplifies needed isolation. Available in 20-pin 0.3" plastic DIPs and SOICs.

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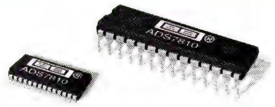

New 12-Bit, Low Power, 800kHz Sampling A/D

ADS7810's 800kHz sampling rate makes it the world's fastest, 12-bit, monolithic SAR ever—60% faster than its closest competitor! Its high speed, small size, low power, low cost, and excellent Nyquist performance make it ideal for data acquisition, DSP boards, and image processing/scanning applications. Key specs include: 800kHz min sampling rate, 12 bits resolution, 70dB min SINAD with 250kHz input, ±0.5LSB max INL, ±0.9LSB max DNL, and 250mW max power dissipation. Available in 28-pin 0.3" plastic DIP, SOIC and die.

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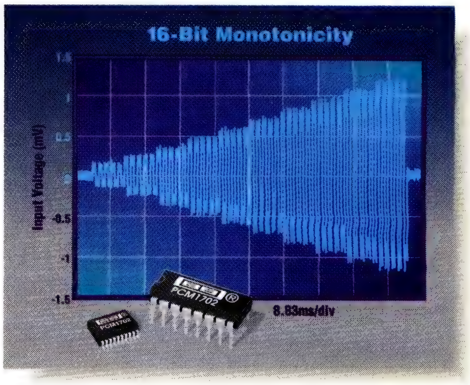

20-Bit BiCMOS DAC

PCM1702's unique architecture produces a 20-bit DAC with high dynamic range, high SNR, and very low distortion. Processed using BiCMOS technology, it has very low power consumption and is packaged in a compact 16-pin plastic DIP or 20-pin SOP. PCM1702 is an unbeatable choice for high-end CD players, musical instrumentation and professional audio applications. Key specs include: –96dB max THD+N, 104dB typ dynamic range, 110dB typ SNR, 200ns typ settling time, and 150mW typ power dissipation.

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New

+5V Voltage Reference Guarantees Long-Term Stability

REF05 is a precision +5V voltage reference that's a pin for pin replacement for the industry standard REF-05. Its guaranteed long-term output voltage drift of 25ppm/10 hours max is 4 times more stable over extended use than the closest competitor. Key specs are: +5V ±0.1% max output voltage, 8.5ppm/°C max temperature stability, 10μVp- (0.1Hz to 10Hz) noise, 0.008% max line regulation, 0.005%/mA max load regulation, 1.4mA max quiescent current, and 8VDC to 40VDC supply range. Available in an 8-lea hermetic TO-99.

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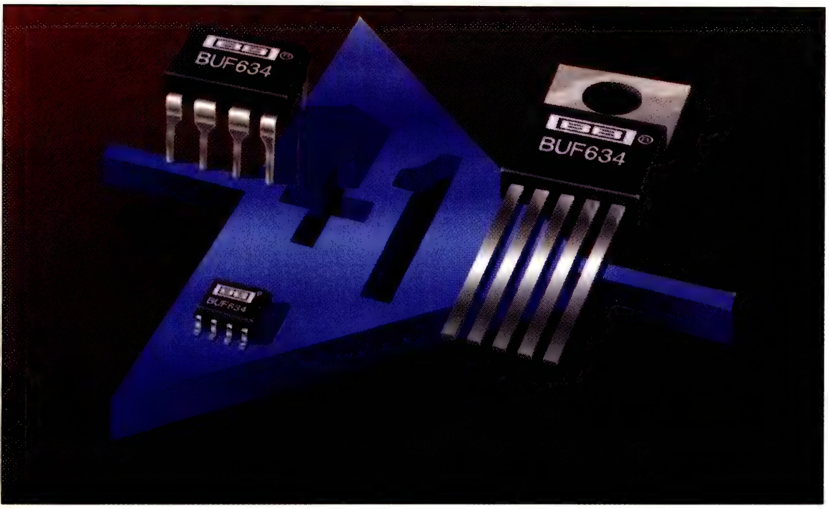
New Product Update



New 250mA Buffer Amp Slews at 2000V/μs

BUF634 is a high speed, unity-gain buffer amplifier that delivers 250mA output and 2000V/μs slew rate—all in a tiny SO-8 package. Its low price, high performance, rugged monolithic design, and ease of use make BUF634 ideal for a wide range of general purpose applications. It's an excellent driver for valves, solenoids, video, and even headphones. BUF634 comes in three different packages: an SO-8 surface mount, an 8-pin plastic DIP, and a 5-pin TO-220.

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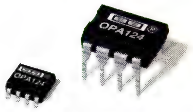
New



Low Noise, Precision *Difet*® Op Amp

)PA124 is a precision, monolithic FET op amp hat delivers low bias current, noise, voltage)ffset, and drift plus high open loop gain nd common mode rejection. Its versatility, mall size, and low price make it ideal for nalytical and laboratory instrumentation, data cquisition, test/medical equipment, and optolectronics. Key specs include: 6nV/$\sqrt{Hz}$ 10kHz) voltage noise, 1pA max bias current, μV/°C max drift, 120dB min open loop gain, 00dB min common mode rejection, and 50μV max offset. Available in compact 8-pin urface mount and plastic DIP packages.

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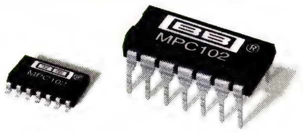

2 x 1 Dual, Video Multiplexer

MPC102 is a dual, 2 x 1 signal multiplexer that distributes and routes wideband analog and digital signals at a high data rate. Designed for high-definition television and broadcast equipment, its excellent harmonic and dynamic specifications are also ideal for radar, communications, computer graphics, and data acquisition systems applications. Key specs include: 210MHz (1.4Vp-p) bandwidth, 640V/μs (2Vp-p) slew rate, 68dB channel crosstalk (30MHz), +6mV/–8mV switching transients, and ±4.6mA (one channel)/±230μA (no channel) quiescent current. Operating from a ±5V supply, MPC102 is available in 14-pin DIPs, SOICs, and dice.

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New Linear Products IC Data Book

The Linear Products IC Data Book contains complete product descriptions, specifications, applications tips, and ordering information for a broad line of high performance, high quality linear products. Its 1100+ pages give designers more than 30 new high performance linear ICs. New products profiled include: operational amplifiers, instrumentation amplifiers, isolation products, power operational amplifiers, references, regulators, and demonstration boards. The Linear Products Data Book is **FREE** from any Burr-Brown sales office or representative.

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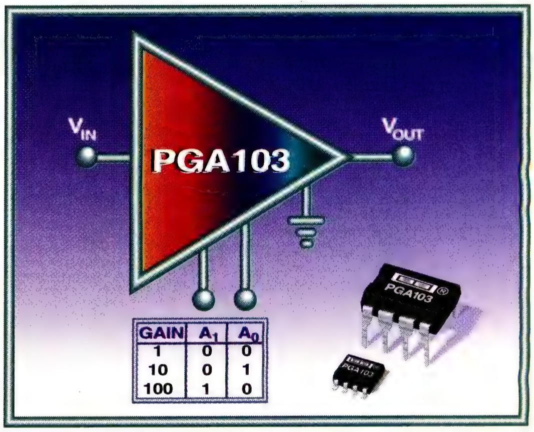

New "Easy-to-Use" Programmable-Gain Amplifier

PGA103 is a monolithic digitally programmable amplifier available in an 8-pin plastic DIP and SO-8 surface mount packages. Gains of 1, 10, and 100 are digitally selected by two TTL- or CMOS-compatible control lines. It's an "easy-to-use" simple solution for systems that handle wide dynamic range signals. PGA103's precision, versatility, size, and low cost make it ideal for process control, medical instrumentation, test/measurement equipment, and general-purpose analog boards. Dice also available.

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0150 is an ultra high-speed capacitively coupled digital device that provides high isolation with very low power consumption. Designed to replace optocouplers, its low power, high eed, and low cost make it a reliable alternative. Use it for A/D and D/A conversion, multiplexed data transmission, computer-to-peripheral interfaces, I/O port isolation in instruments, wer inversion, and isolated data acquisition systems. Key specs are: 80M Baud typ data rate, TTL/CMOS compatibility, 25mW max power consumption per channel, tested at 00Vrms isolated partial discharge per VDE0884, and 16.5mm creepage distance. Available in 24-pin single-wide plastic DIP.

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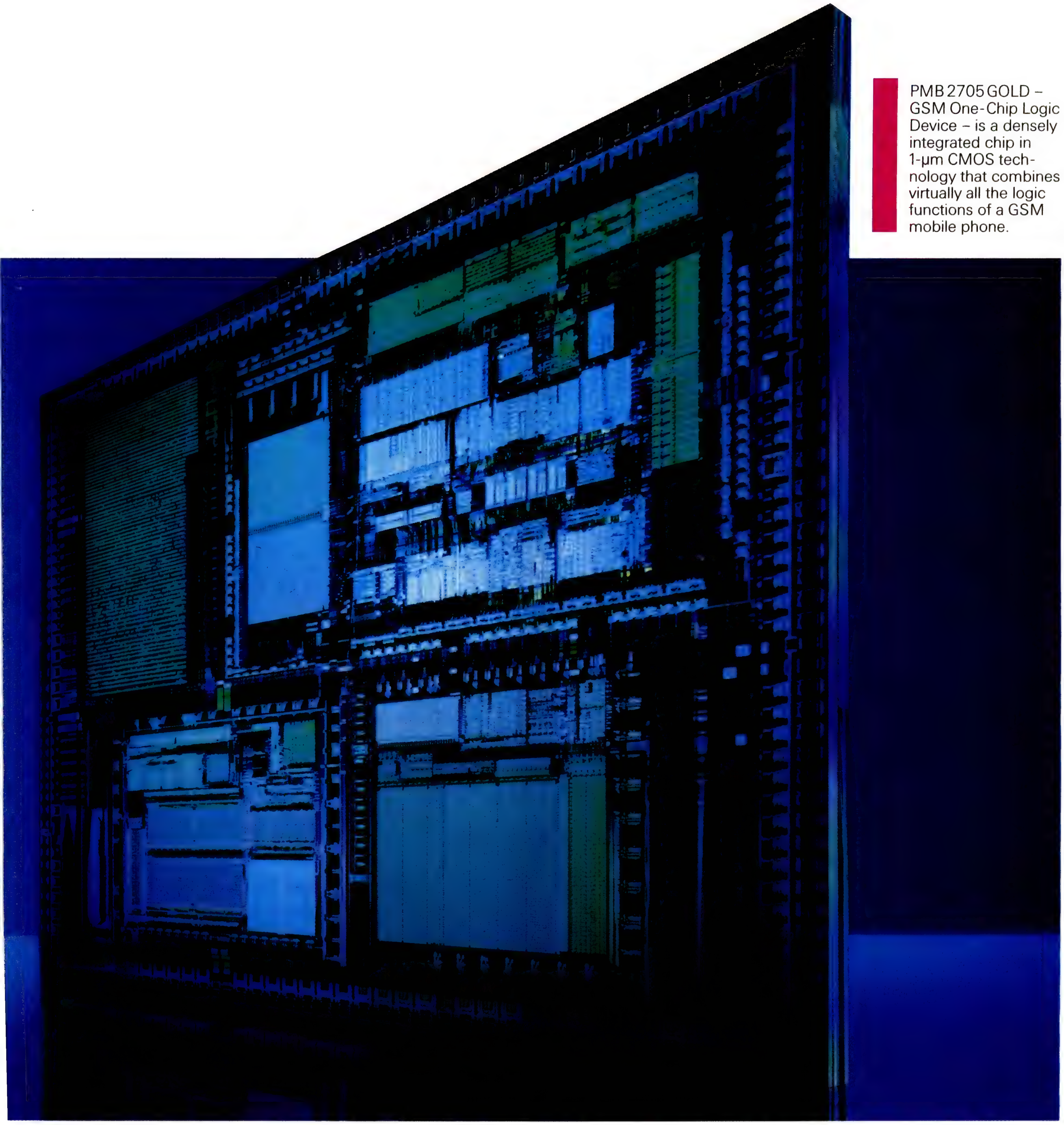

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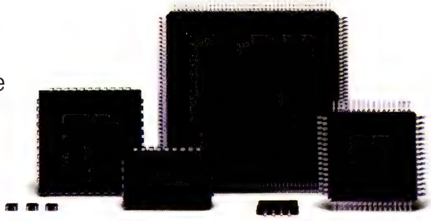

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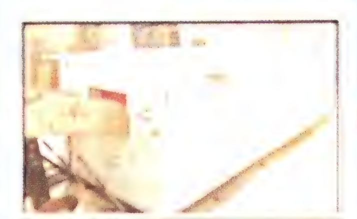

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TECHNOLOGY NEWSLETTER

FERROFLUIDS IMPROVE STEPPING MOTORS

Adding ferrofluids to the air gap of a permanent-magnet stepping motor will dramatically improve the motor's performance. For instance, settling time of a motor step is decreased by a factor of seven, motor and shaft vibrations and acoustic noise are significantly reduced, and resonant instability is minimized. The natural lubrication properties of the ferrofluid also greatly extend motor life. Moreover, the fluid saves space by eliminating the need for external friction-type dampers. These results were discovered through a joint effort between motor manufacturer Eastern Air Devices, Dover N.H., and ferrofluidics technology leader Ferrofluidics Corp., Nashua, N.H. Ferrofluids, which can be controlled by magnetic fields, consist of microscopic magnetic particles immersed in a stabilizing agent. The motor's permanent magnet naturally retains the fluid, eliminating the need for mechanical seals. High slewing speeds, plus high-acceleration, shock, and vibration levels can't dislodge it. A high-precision, bidirectional size-23 stepper is the first motor to employ the ferrofluids. It combines 1.3°-step angles with ±3% noncumulative positioning accuracy. And that's without negative position feedback, since torque ranges are held from 40 to 200 oz.-in. The motor is available with windings for either a 4-phase unipolar drive or a 2-phase bipolar drive. For additional information, call (603) 742-3330. *FG*

U.S. NAVY FUNDS SILVER-ZINC RESEARCH

Improvements in the cycle life, wet life, and energy density of silver-zinc rechargeable batteries are the goal of a two-year Phase II R&D program funded by the U.S. Navy. The recipient of the award, Yardney Technical Products Inc., Pawcatuck, Conn., will seek to leverage its electrode-coating process to enhance the zinc electrodes and separators. The silver-zinc cells are of interest to the Navy for applications requiring high discharge rates, small size, light weight, high power output, and long cycle life. The research contract was awarded by the Naval Surface Warfare Center, White Oak Laboratory, Silver Spring, Md., under the Small Business Innovation Research program. *DM*

PORTABLE SYSTEM GIVES THE SPEECHLESS A VOICE

A helmet-mounted vision-tracking system, combined with a wheelchair-mounted personal computer, allows people with disabilities to "speak with their eyes." The system employs a video camera to track the position of the eyes' pupils as the wearer looks at words, pictures, letters, and other symbols on a clear screen. Both the camera and screen are mounted on the helmet. The system was developed by Lester Gerhardt, associate dean of engineering, and Ross Sabolcik, a graduate student, of Rensselaer Polytechnic Institute's Center for Advanced Technology in Automation and Robotics. The screen symbols represent simple requests, words, or even letters or phonemes that can build words. Various symbols are available because users can change screens by looking at the appropriate symbol. A teacher or caretaker can add words or pictures to customize the screens. The digitized picture of the pupil is sent to the computer, which can produce a synthesized sound—or control the wheelchair or other equipment. Although the basic idea isn't new explains Gerhardt, "advances in computer technology and a new approach have let us create a relatively inexpensive portable system that is not affected by most head movements and is tolerant of variations in lighting." Contact Lester Gerhardt at (518) 276-6400. *JN*

INPUT BY BRAINWAVES MAY OBSOLETE KEYBOARDS

With the help of digital-signal-processing technology and brainwave training software, controlling a computer by brainwaves has moved beyond science fiction. The BrainLink interface passively detects brainwaves via a series of sensors attached to a headband worn by the user, similar to an electroencephalogram (EEG). After amplification, the signals are digitized. Built around a Motorola 56000 DSP chip, Advanced Neurotechnologies' (Colorado Springs, Colo.) system converts time-domain brainwave signals to the frequency domain using a high-resolution fast Fourier transform (FFT). The interface relies on a proprietary protocol that extracts relationships of brainwave activity that can be learned and directed by the user. The protocol discriminator analyzes the amplitude and phase relationships between multiple subhertz-frequency ranges. A proprietary algorithm features normalization, autoranging, equalization, windowing, and comparison of subhertz-frequency amplitudes and phases. Besides training individuals and groups, the company is licensing the aNi protocol and Brainlink system. Contact aNi's Richard Patton at (800) 841-1326 or (719) 578-9323; fax (719) 578-1147. *SVT*

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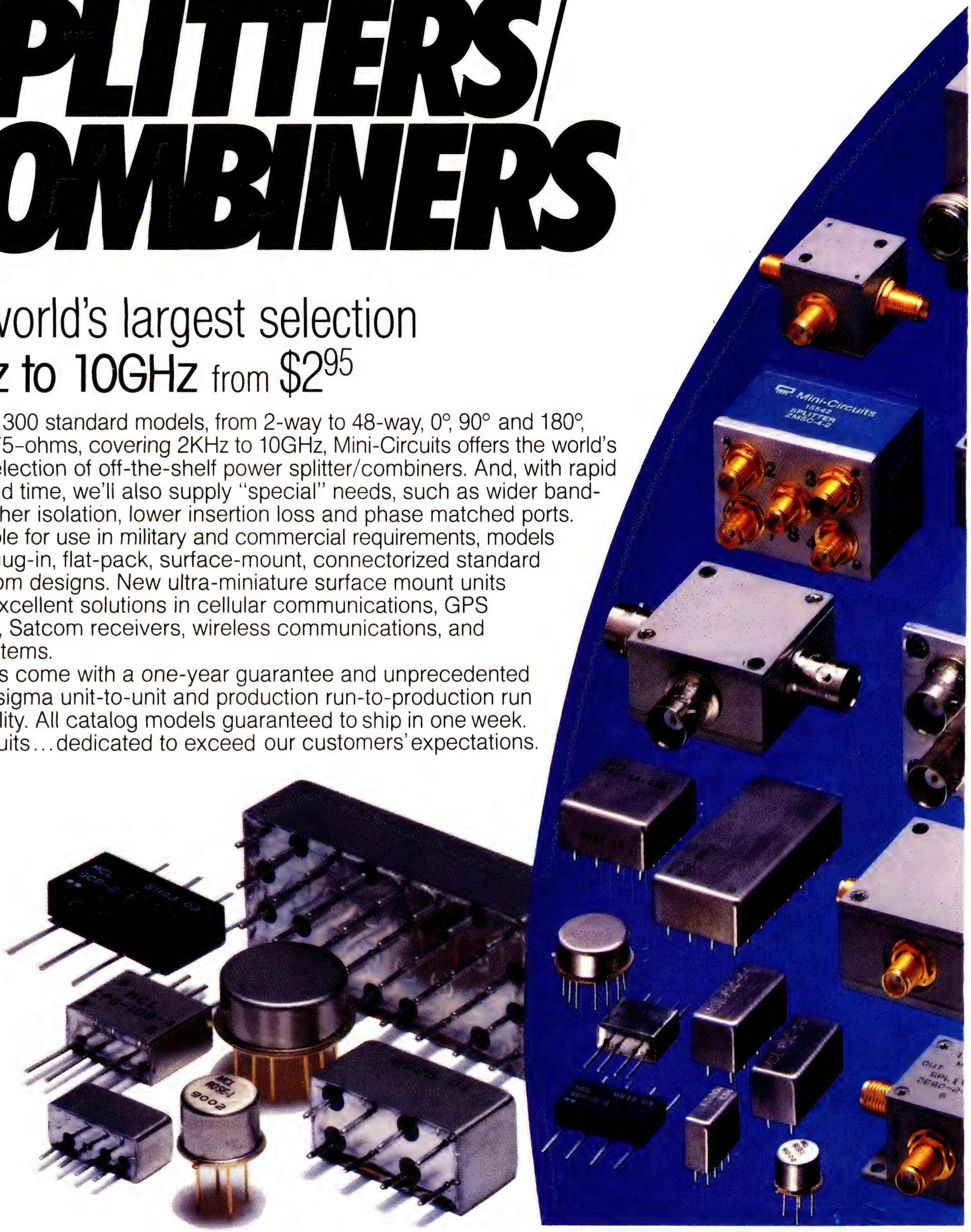

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F134 Rev D

TECHNOLOGY NEWSLETTER

ENHANCED STANDARD IMPROVES ETHERNET LANs

An enhancement being developed for the Ethernet telecommunications protocol will permit existing Ethernet LANs to support real-time, multimedia applications while maintaining compatibility with existing services. Based on 10Base-T Ethernet, the isoEnet standard is a segmented, switched protocol that adds 6 MHz of bandwidth to each node in the hub in the form of 96 switched ISDN-type B channels (64 kbits/s). These channels can be used separately or concatenated to provide variable-bandwidth data paths for voice, video, or high-speed data transfer. This 60% increase in data-channel capacity is achieved by changing the encoding of the Ethernet signal from Manchester to 4B/5B, thus significantly reducing the bandwidth overhead. Because 4B/5B encoding can't be used by conventional Ethernet equipment, the isoEnet protocol will automatically determine the encoding scheme used by a channel and employ the appropriate one. Because the hub technology can support a mixed environment of both normal and enhanced Ethernet, LANs can be upgraded as needed on a node-by-node basis. No upgrades to existing wiring are required, and the per-node costs for LAN hardware supporting the enhanced service will most likely cost only 25% more than standard service equipment. Establishment of this protocol as an IEEE standard is well underway, with work nearly complete by the IEEE 802.9 standards committee. Industry support for isoEnet, originally developed by National Semiconductor, Santa Clara, Calif., is already on the rise. A number of companies, including Luxcom, Erickson, IBM, Apple, and Xidicron, have isoEnet-capable products under development. For more information, contact National Semiconductor's representative Christopher Koehle at (408) 721-7763. *LG*

JOINT EFFORT HOMES IN ON CVD TiN PROCESS

Attempts to develop a production-worthy process for the chemical-vapor deposition of titanium nitride (CVD TiN) at low temperatures are now being initiated at Novellus Systems Inc., San Jose, Calif., and Sematech, Austin, Texas. The joint development program will support the requirements of Sematech's advanced semiconductor manufacturing applications. Researchers will focus their attention on demonstrating the process, particle, and reliability performance of Novellus' CVD TiN system. The CVD TiN system, being developed on the company's Concept Two modular platform, complies with Sematech's SEMI MESC specifications. The final process will be used for Sematech's research program, which demonstrates advanced manufacturing capabilities to generate the 0.25-μm IC-device. The process will probably be introduced sometime this year. For more information, contact Novellus' Thomas Bowman at (408) 943-9700. *CA*

SOUPED-UP PENTIUM RUNS AT 100 MHZ AND 3.3 V

By moving the Pentium processor design to a 0.6-μm biCMOS process and four levels of metal, designers at Intel Corp., Santa Clara, Calif., were able to increase internal operating frequency to 100 MHz. That lets the chip deliver close to double the throughput of current-generation Pentium processors. At the internal 100-MHz clock speed, the chip will dissipate only about 4 W—a four-fold decrease in power consumption over the 5-V, 66-MHz version. The power reduction was achieved by using finer-line lithography, reduced parasitics due to the smaller chip size, and more aggressive internal power management. Although the processor was described at last month's ISSCC in San Francisco, Calif., Intel indicated it would not release the 3.3-V version (internally referred to as the P54C) until late 1994 or early 1995. However, those plans have changed. Now the 3.3-V Pentium with internal clock speeds of 90 or 100 MHz will be unveiled this month. The new CPU will include extra features so that it can be used in multiprocessor systems. To support the new high-speed processors, Intel is developing an upgraded motherboard chip set code-named Neptune. It will support dual processors, plus the higher 50-MHz bus speeds. The basic chip set supports ISA buses; by adding one more chip, it also can support EISA buses. *DB*

DIAMOND FLAT-PANEL PHOSPHORS STUDIED

Research into perfecting color phosphors and screens for a new generation of diamond thin-film flat-panel displays will shift into high gear thanks to a recently reached agreement. Under the agreement between SI Diamond Technology, Houston, Texas, and the David Sarnoff Research Center, Princeton, N.J., the research center will investigate the appropriate color phosphors to interface with SI Diamond's field-emission displays (FEDs) to ensure the desired brightness, contrast, and operating-life levels. In addition, Sarnoff will assist SI Diamond in such issues as display-screen size and resolution. Unlike current FEDs, whose color screens are based on zinc-sulfide phosphors that contaminate the display's silicon and metal microtip cathodes, FEDs using diamond cathodes are contamination-free. The diamond material's inert qualities make it resistant to the sulfur. For more information, contact SI Diamond's Marijane Ensminger at (713) 529-9040. *RA*

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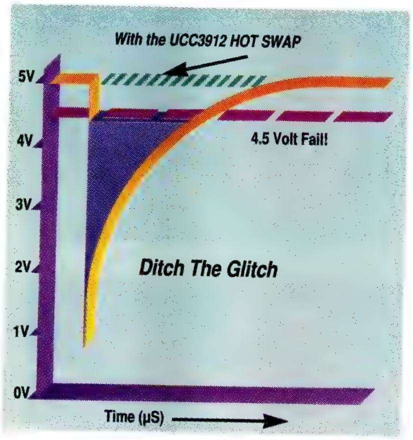

The UCC3912 Advantages

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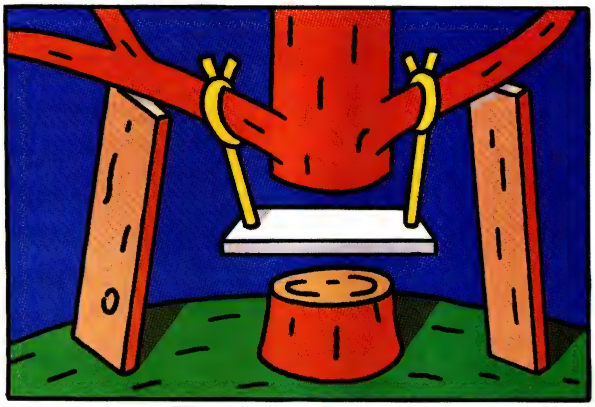
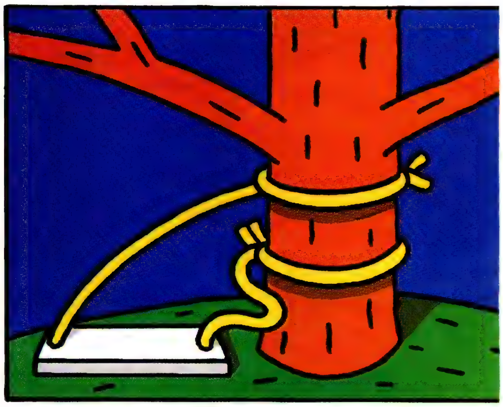
READER SERVICE 177

Xilinx FPGAs.

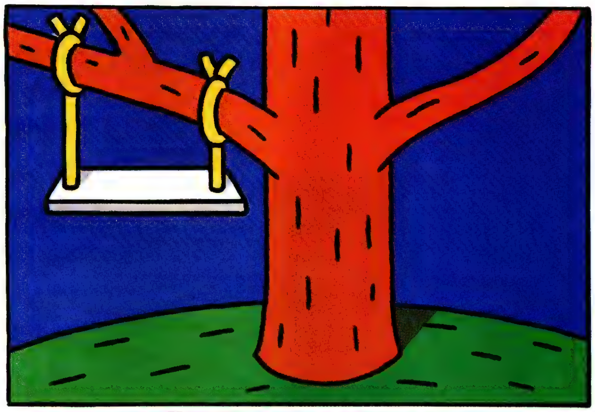
The perfect parts for an imperfect world.



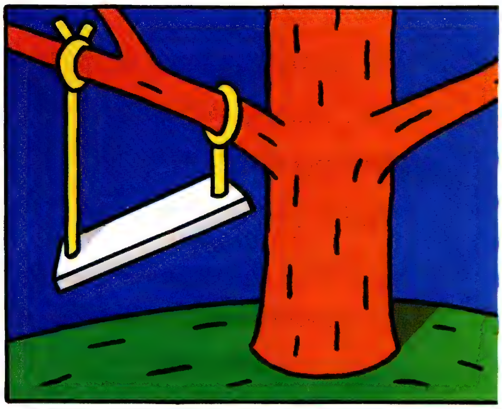
What Marketing Asked For



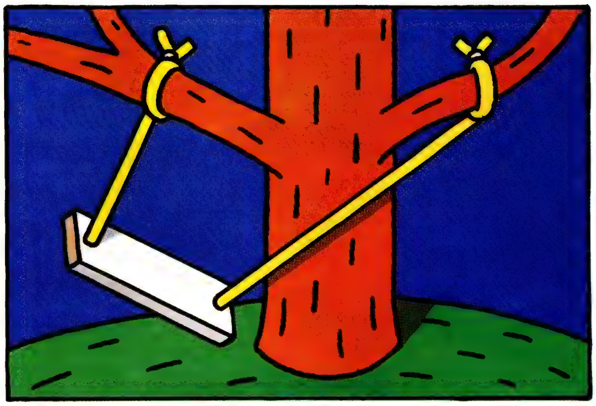
What Design Specified



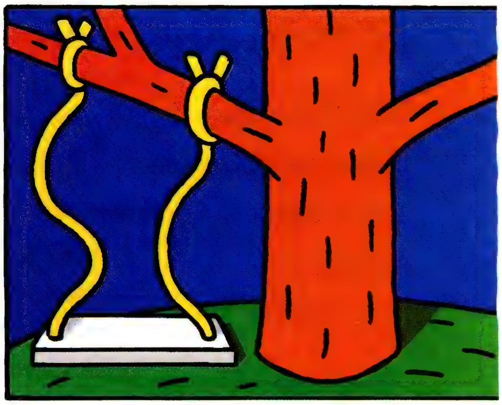
How Manufacturing Built It



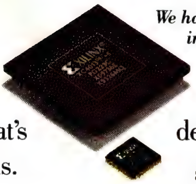
What QA Approved



What Engineering Developed



What Documentation Described



We have as many options as you need (more than 350, in fact), from our new 13,000 gate XC4013 FPGA, to our space-saving TQFP.

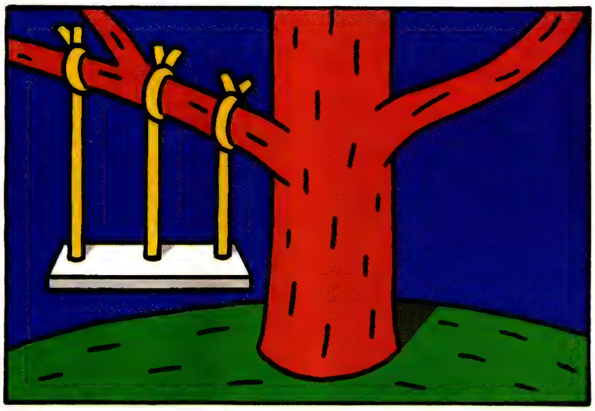
Look familiar?

We're willing to bet a sizable chunk of next week's pay that a cartoon like this hangs in just about every engineering department in this country.

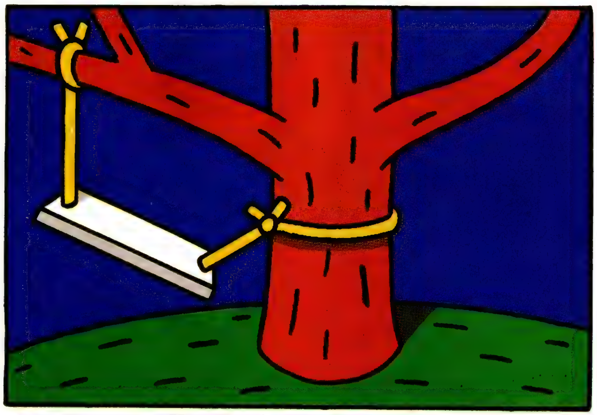
Why?

Because that's just the way it is.

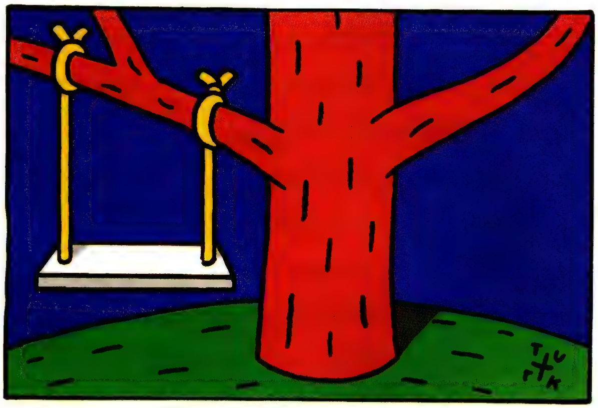
So given the amount of miscalculation, miscommunication, and misdirection you have to deal with, why not choose a logic device that won't let you go wrong?



What Management Agreed On



How Marketing Changed It

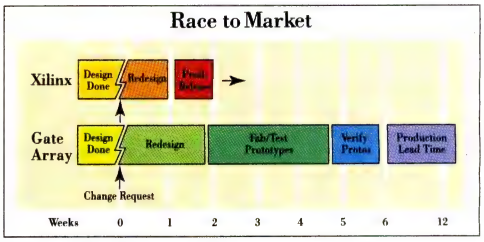


What The Customer Wanted

Nothing does that better than an FPGA from Xilinx.

First of all, since we make more than 350 different speed grades, densities, and packages, you can get off to a flying start with just the right part.

Then, with our powerful XACT™ Development System, you can work with your design down to the gate level if necessary, to get it right, right off the bat.



With FPGAs from Xilinx, you can get to market faster even if you make a ton of changes — all in less time than a single gate array change cycle.

But even if you can't get your first design to fly (or the guys in marketing change their minds), there's no problem. You and your colleagues can go back and forth as often as you like.

Because you can change a Xilinx FPGA as often as you like, with no hard feelings. And no added expense.

In fact, you can even make changes right in the system, because our devices are reprogrammable.

And since Xilinx FPGAs are never actually changed—just programmed—they won't hang you with too much inventory—or worse—not enough.

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A better question might be, What will it cost you not to have it?

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READER SERVICE 198

Soar to success aboard ultra-fast Bipolar and BiCMOS carriers

Incessant demands for higher speed. That's the challenge for designers of testers, telecom products, high-end workstations and image processing systems. And now there's a way to rise above it—with NEC's 0.5-micron ASICs featuring ultra-fast Bipolar and BiCMOS technologies.

For 1.2GHz applications, our ECL-8 gate array family offers the highest speeds in the industry: 50ps* basic gate delay and 153ps** fully loaded. The family also offers the world's highest density: 68K gates (full-adder equivalent gates). An ECL-8 master with 23K gates is also available.

The family has a library of more than 100 internal function blocks. These blocks offer optimum power-speed solutions for diverse applications. There are three modes of current switching and five modes of emitter-follower circuits, including an enhanced active pull-down mode.

For fast answers, call us at: USA Tel:1-800-366-9782. Fax:1-800-729-9288. Germany Tel:0211-650302. Fax:0211-6503490. The Netherlands Tel:040-445-845. Fax:040-444-580. Sweden Tel:08-753-6020. Fax:08-755-3506. France Tel:1-3067-5800. Fax:1-3946-3663. Spain Tel:1-504-2787. Fax:1-504-2860. Italy Tel:02-6709108. Fax:02-66981329. UK Tel:0908-691133. Fax:0908-670290. Ireland Tel:01-6794200. Fax:01-6794081. Hong Kong Tel:886-9318. Fax:886-9022. Taiwan Tel:02-719-2377. Fax:02-719-5951. Korea Tel:02-551-0450. Fax:02-551-0451. Singapore Tel:253-8311. Fax:250-3583. Australia Tel:03-8878012. Fax:03-8878014. Japan Tel:03-3454-1111. Fax:03-3798-6059.

I/O macros include interfaces for ECL-100K, ECL-101K and ECL-10KH.

We'll add a new master with an embedded BiCMOS SRAM in March. The 1K x 40-bit memory features an access speed of 2.8ns (max).

For 156MHz applications, choose the CL series of our BiCMOS-8 gate array family. The CL series features 180ps* CMOS/BiCMOS logic and compiled BiCMOS RAM with 8ns cycle time (max). Four masters cover the range from 11K to 165K usable gates. Interfaces are ECL-100K, 10KH, LVTTL and GTL.

For 622MHz applications, we'll introduce the CEL series with ECL logic in May.

If you want your system to soar above the competition in a speed-intensive market, call NEC and ask about our Bipolar/BiCMOS gate arrays, today.

*F/0=1, L=0mm **F/0=3, L=3mm

NEC

READER SERVICE 117

Save the Earth

and board space.

You can do it all with the nvSRAM.

If you are using lithium batteries to back up your SRAMs, there's something you should know. Lithium batteries can harm the environment. They can corrode, leak, explode, and produce poisonous gas.

If this concerns you, take a look at Simtek's nonvolatile SRAM — the nvSRAM. No battery is needed to back up data when power is removed, which means there's no battery to throw away when it fails. When you use the nvSRAM, you can feel good about doing your part to help clean up the environment.

We realize, however, there's more to choosing nonvolatile RAM than environmental and safety considerations. Let's talk performance. Without a battery to fail, reliability is unsurpassed. And imagine what you can do with the board space you'll save. The density and speed you need — 64K (with 256K on the way) and access times to 30ns — are there, too. Along with a price that's welcome in any system.

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READER SERVICE 131

HOLOGRAPHIC STORAGE TECHNOLOGY EDGES ONE STEP CLOSER TO REALITY

A storage system based on holographic technology has made it possible to record several bright, erasable holograms in the same spot, using photorefractive polymer films. This feat, previously only possible employing expensive crystals, has brought a great deal of attention to the study of holography as a potential data-storage system.

Holography's success in the storage field hinges on its ability to optically store large amounts of information as holograms in very small volumes. It also must be able to record and project images with access times and data rates much faster than magnetic hard-disk drives.

Magnetic and optical systems have long dominated the storage market. However, an increased demand for significantly more storage capacity coupled with the development of a wide variety of applications have taxed the ability of these storage systems. And, as the requirements on these systems continue to grow, the limits on current technology will eventually be reached.

One solution, as identified by the researchers from the IBM Research Division, San Jose, Calif., is a holographic storage system. This system, in contrast to conventional magnetic and optical recording, requires the unique integration of many different technologies as opposed to one dominant technology. By combining these technologies, it's anticipated that the resulting storage system would be both original and competitive in performance, size, and cost. Researchers believe that such a system could even potentially have access times and data rates 100 to 1000 times faster than today's magnetic hard disks. One of the key features of holographic storage is its ability to store information redundantly. The storage process involves two basic steps: first storing an interference pattern from a range of data, and next retrieving this stored information at a later date *(Fig. 1)*.

Information recorded using conventional technologies occupies a discrete location in or on the recording layer. In contrast, a bit recorded by holographic means is stored in the form of an interference pattern that spans the entire area or volume of the hologram.

The storage process starts by forming a two-dimensional page of digital information on a spatial light modulator (SLM). The SLM is illuminated by a laser beam, resulting in a transmitted light or signal beam. Both the signal beam and a reference beam of light are then directed at the same spot on the recording medium. The intersection of the beams produces an interference pattern that's recorded as a hologram. Numerous holograms may be recorded in the same spot by either changing the angle with respect to the recording medium of the sample or the laser beams for each individual hologram.

Because a single page of bits may be stored at one time, the information content of the page is intermingled. Thus, any defect occurring in the recording medium would not destroy the data bits. Rather, the signal level of all the bits would be reduced.To retrieve the stored information, the recorded hologram is illuminated with a replica of the reference beam. This effectively creates a replica of the original signal beam. That beam is then used to form an image of the original SLM data pattern on an array of photodetectors.

In conventional storage, data is recorded and retrieved serially. Holographic storage, on the other hand, uses the information capacity of an optical wavefront so that data can be recorded and retrieved in parallel, one page at a time. Due to the page-oriented nature of holographic storage, the potential exists for extremely high data rates, subject only to the limitations imposed by I/O devices. In simpler terms, holographic storage systems should have data rates approaching 1.0 Gbytes/s. In addition, because beam deflection, as opposed to moving parts, is used to access the stored holograms, access times in the 10-ms to 10-ms range could be achieved.

Holographic storage also lends itself well to multiplexing. In this process, the holographic structure of one page is intermixed with the holographic structures of other pages. Hence, multiple, independent pages of data can be recorded at the same spot on a relatively thick recording layer. In effect, if multiple holograms were stored in increments of 0.9 nm on a recording medium approximately 1.0 mm thick, then a total of 500 holograms could be stored in one location. Thick recording layers also help minimize the number of defects tolerated. Consequently, multiple pages of data may be retrieved with minimum crosstalk.

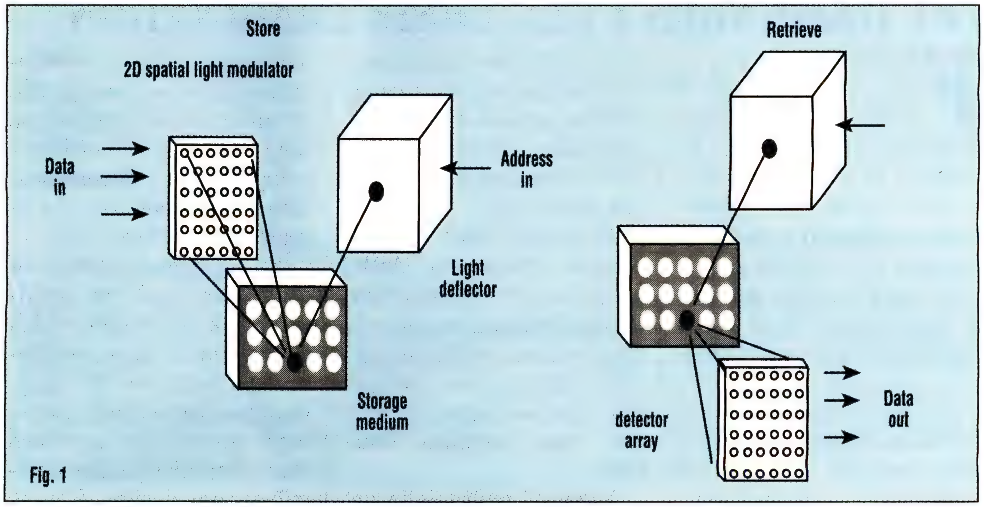


Fig. 1

Current holographic storage systems require the use of high-performance-grade components *(Fig. 2)*. Optimum performance necessitates that many of these components be pushed beyond their current performance capabilities. Nevertheless, although it could be up to 10 years before a completed holographic storage system is ready to ship, great progress has been made in many of the key system components.

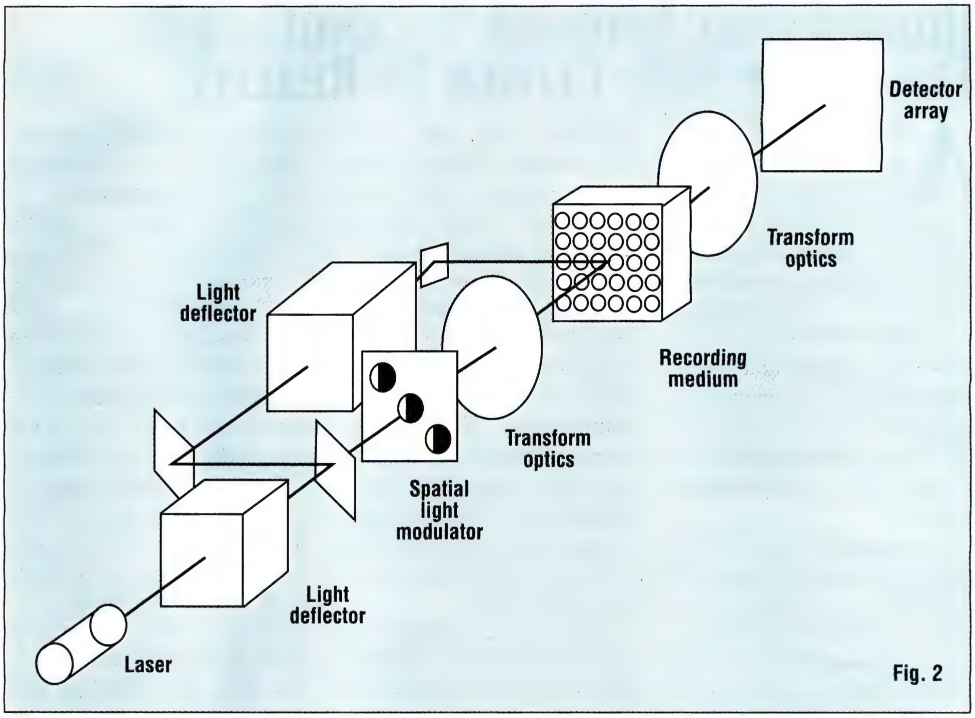


Fig. 2

Recent developments in the area of integrated CCD arrays have replaced discretely mounted photodiodes. For instance, liquid-crystal SLMs have supplanted photographic masks and film transports. Also, efficient laser diodes, which can be used directly or as pumping sources to provide blue-green light, have been developed. With these devices, holographic technology is able to gain more attention as the potential storage technology of the future. However, the technology is still in its evolutionary stages. To achieve a complete understanding of the technology's capabilities and the requirements it will need to meet will require further study.

Despite all of the advances made over the past few years, several issues have impeded the successful implementation of holographic storage. Most important has been the lack of a suitable material system. Unfortunately, identifying this material is not as easy as it sounds. The numerous storage applications, each with their own requirements, make it virtually impossible to single out one particular material.

Yet, with the recently renewed interest in holographic technology, researchers are more hopeful that not only will they identify a material system, but integrate it into a workable holographic storage system. It's hoped that such a system will one day surpass today's technologies in terms of cost and performance. By some estimates, real industry impact from this technology could be as close as five years away.

For further information, contact the IBM Research Division, Almaden Research Center, 650 Harry Rd., San Jose, Calif.; 95120-6099.

CHERYL AJLUNI

BUILDING BLOCKS, ALGORITHMS FOR MULTIMEDIA LET DESIGNERS FLEX THEIR IMAGINATION

Flexibility—the key to any designer's bag of tricks—has long been aided by standard-cell libraries. In the multimedia-system domain, such flexibility is stressed to the limit because of evolving standards and the many pockets of opportunity, from video conferencing to home theaters and much more. However, to maximize design capabilities, engineers need a library of cells optimized for multimedia applications. These cells are used to create building blocks, such as codecs, motion estimators, quantizers, discrete cosine transforms, entropy encoders, and others.

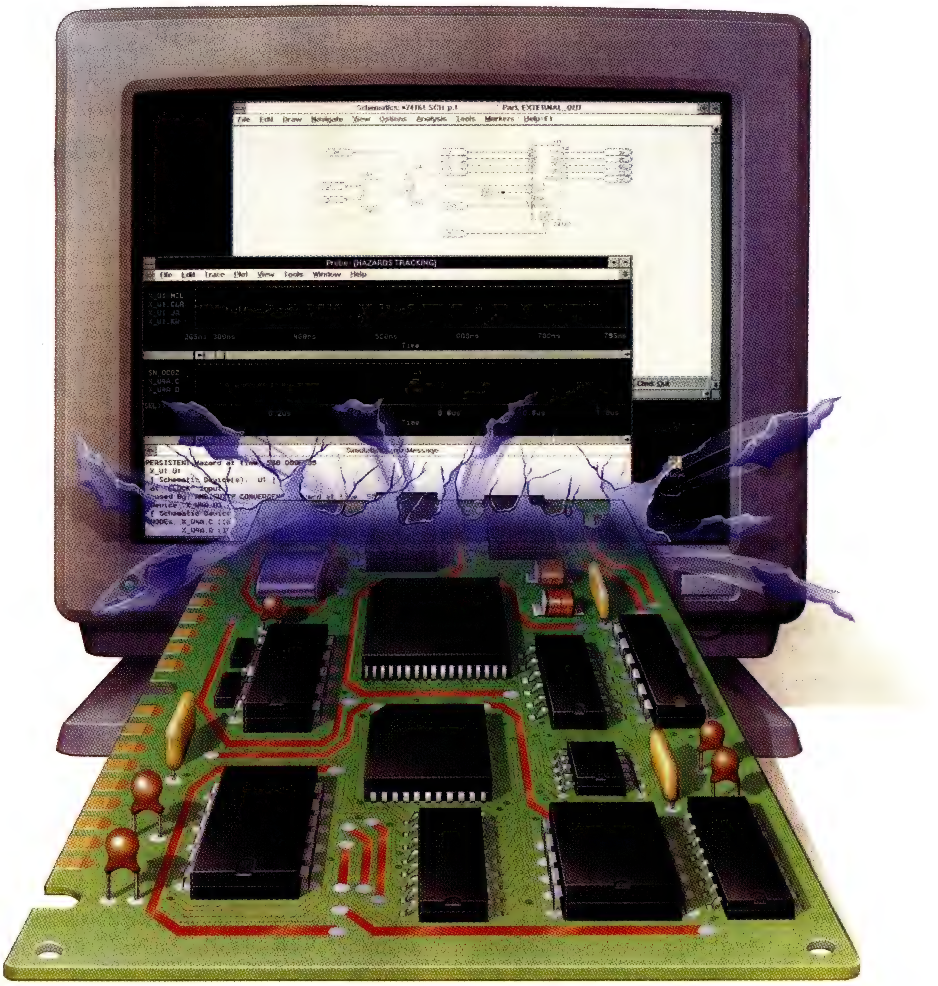
Although most cell libraries offered by ASIC suppliers often include hundreds of cell options, most of these cells are relatively generic. That leaves designers with having to develop the more complex functions.

Much of multimedia design, however, is in the algorithm more so than in the circuitry. Thus, algorithms hold the key to efficient compression, decompression, and other aspects of multimedia subsystems.

By combining a family of algorithms and the building-block cells with which to implement them, designers at CompCore Multimedia Inc., Santa Clara, Calif., came up with an approach that simplifies multimedia-subsystem design. Key to the CompCore scheme is a family of highly efficient algorithms that can implement key standards, such as Px64 for video conferencing or MPEG-1 and MPEG-2 for still and motion video, with minimal logic. Furthermore, the algorithms are highly portable and can be implemented in any ASIC-supplier's process to become part of that company's cell library.

The initial library of functions offered by the company includes a number of key building blocks for the task of video decompression—a Huffman decoder,

Finally...



Digital Analysis You Can Use!

If you are a designer who works on real-world digital circuits, you need an EDA system that allows you to efficiently verify and debug your design. The Design Center desktop EDA system with the **PLogic** digital circuit simulator provides the features you need.

- Digital worst-case (min/max) timing analysis helps you find timing problems in your design using the range of delays specified by the manufacturer. This technique can find problems that simple single-delay methods can't—even with multiple runs.
- When there are problems with your design, such as setup/hold or worst-case timing violations, the Design Center eliminates the guesswork. Detailed warning messages lead you directly to the timing errors; interactive capabilities help you automatically associate selected messages with corresponding waveforms.
- The Design Center's unencrypted libraries offer over 1,800 off-the-shelf digital devices including TTL, CMOS, 10K and 100K ECL, and PLD devices. All of this at no extra cost! You can also easily model new devices directly from specifications provided in data books. **PLogic** supports pin-to-pin delay specifications, timing constraints, and logic expressions, as well as a wide variety of low-level primitives.
- If you design with standard or complex PLDs, the Design Center with PLSyn provides you with fully integrated device-independent logic synthesis. Design and simulate using any mixture of programmable logic and discrete digital parts. Then, let PLSyn automatically partition and fit your programmable logic into one or more parts of your choosing.

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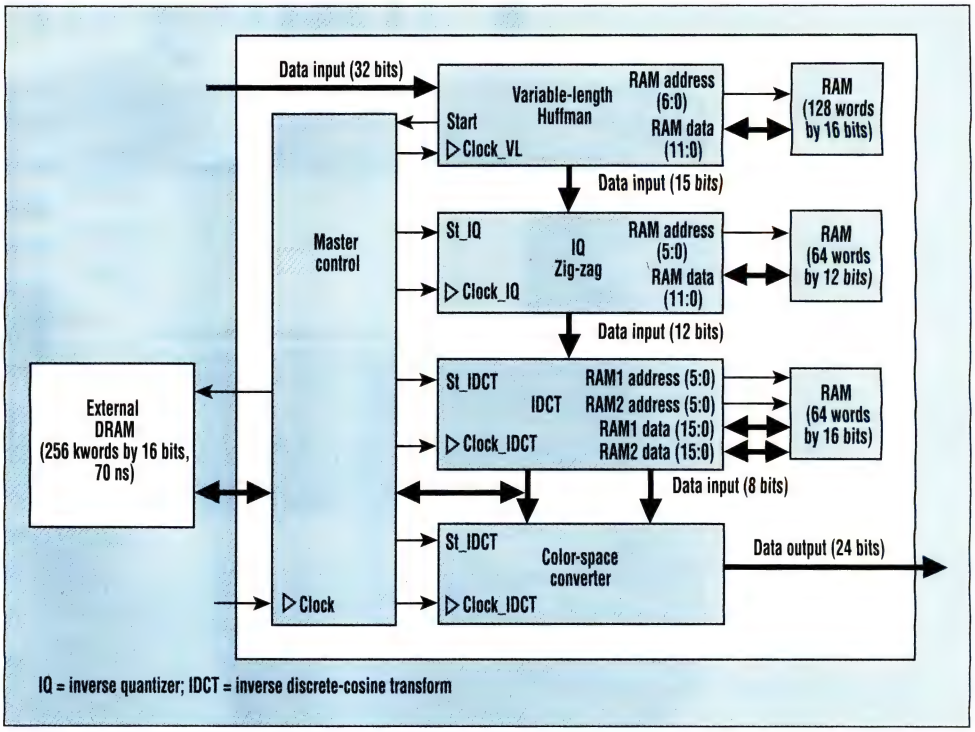
an inverse quantizer, an inverse discrete cosine transform, a motion estimator, and a color-space converter. Designers can combine them to form a complete MPEG decoder and still have room to spare for other functions *(see the figure)*. Or, some of the processing can be done in software on an off-chip processor, minimizing the silicon overhead.



IQ = inverse quantizer; IDCT = inverse discrete-cosine transform

The high efficiency of the algorithms is key to efficient silicon usage. For instance, the Px64 codec designed for video conferencing requires only about 5000 gates of logic plus RAM and can run at a frequency of 20 MHz; an MPEG-1 circuit running at a frequency of 40 MHz needs just 10 kgates plus RAM; and an MPEG-2 implementation at a frequency of 66 MHz uses 18 kgates plus RAM. Such implementations are about three to four times smaller than most other competitive solutions. The inverse discrete cosine transform macrocell, key to many image-manipulation algorithms, consumes less than 2000 gates yet handles an 8-by-8-pixel block size, features a latency of 280 cycles and a throughput of 512 cycles/block, and has precision that's CCITT H.261-compliant.

In addition, the algorithms are implemented using a hierarchical or gate-level, synthesizable, Verilog hardware-design language that can be used with cell libraries from various ASIC manufacturers. By being able to treat each building-block section as an independent block, designers can optimally configure subsystems through typical standard-cell design tools.

Although CompCore doesn't manufacture chips, it will license its algorithms and cell net-list or source-code designs in Verilog or C-language form. This gives ASIC suppliers the opportunity to quickly add multimedia functions to their implementation capabilities. The portable C-software modules for each block can also be used to perform simulations, allowing designers to quickly simulate the subsystem they're designing. That, in turn, minimizes the number of design iterations designers would have to go through.

Companies that expect to implement a large number of multimedia ASICs could also license the library to speed their time to market. By licensing the library, the companies could "shop around" to find the best foundry or set of support/design tools. Licenses for the software library range from about $250,000 for a single-use design, to about $1 million for unlimited use of the library. Although those numbers may seem high initially, as chip production ramps into the hundreds of thousands, the license fee amortizes and adds minimally to the cost of each chip.

For more information, contact George Haber at (408) 773-8310.

DAVE BURSKY

FAST ATA IMPLEMENTATION TRANSFERS DATA AT 13.3 MBYTES/S OVER STANDARD CONNECTIONS

Graphic- and data-intensive applications_interactive multimedia, full-motion video, digital audio, animation, digital photography, and high-resolution graphics_are increasingly finding their way into the mainstream and continue to tax PC buses. In the workplace, desk-to-desk white-board collaboration and video conferencing, workgroup computing, and client-server architectures are all emerging as tools required to maintain office productivity. To support this increase of data handling, a faster method of shuttling data is needed. This is where Fast ATA steps in.

Developed by Seagate Technology Inc., Scotts Valley, Calif., Fast ATA is an advanced implementation of the standard AT Attachment (ATA) interface. It transfers up to 13.3 Mbytes/s using a standard VL-Bus-to-ATA or PCI-to-ATA hardware connection *(see the table)*.

Fast ATA is fully functional and backward-compatible with the ATA interface and retains the ATA's standard features for host connections. It also has three advanced industry-standard defined features.

The first feature is pro-

A 32-macrocell EPLD for the cost of a 22V10? Bob found this to be a rather pleasant surprise.

If you're currently designing with 22V10s or other PALs or GALs, then you're ready for the advantages of Altera's EPM7032. Here's a device that triples the density of what you're currently using; saving board space and decreasing power consumption. With pin-to-pin delays as fast as 7.5 ns, you'll be able to support even the fastest Pentium designs. But the real value is that you get these powerful, high-performance features for less than the cost of a 22V10.

To make your move to the EPM7032 an easy one, we're offering our FirstStep design utility, free of charge. FirstStep contains everything you need to automatically convert your existing PALASM and ABEL designs for a no-charge, no-fuss migration to the EPM7032.

When you choose Altera for your programmable logic needs, you get more than speed and density. You also get technology leadership, easy-to-use design software and comprehensive technical support. This is real value. This is the Altera Advantage.

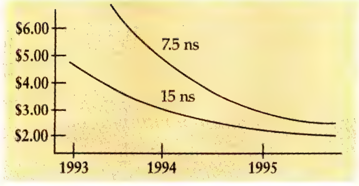
Call us now, at 800-9-ALTERA (800-925-8372) to receive your free copy of FirstStep. You'll find moving up to the EPM7032 will cost less than you ever thought possible.

Now, isn't that a pleasant surprise?

Feature for feature, Altera means value.

	EPM7032	22V10
Macrocells	32	10
Pin Count	44	24
Package Options	PLCC PQFP TQFP	PDIP PLCC
Tpd = 15.0 ns	$ 4.75	$ 7.45
Tpd = 10.0 ns	$ 7.95	$ 9.90
Tpd = 7.5 ns	$11.95	$14.25

Above prices are based on 100 piece quantities. Pricing for the 22V10 is based on the lowest of the published prices from Lattice and AMD as of January 1, 1994.



EPM7032 projected 25,000 unit pricing through 1995.

The ALTERA Advantage

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grammed I/O mode 3, which is the typical BIOS implementation for VL-Bus and PCI connections that deliver 11.1 Mbytes/s in a burst-transfer mode. The second feature is multi-word DMA mode 1, which runs at up to 13.3 Mbytes/s. Multi-word DMA mode 1, which isn't a common implementation, is supported by Fast ATA drives and typically can be found on EISA host-bus connections. The last feature is multiple-block read/write capability. This feature supports increases in transfer rate by up to 30% over standard ATA performance when implemented in BIOS.

However, Fast ATA is more economical to integrate than fast SCSI. Implementing the interface through system BIOS supplies the increased performance without an incremental hardware cost. There's also the added expense of the SCSI interface on a SCSI-based peripheral, such as a hard-disk drive.

On a VL-Bus or PCI system, the Fast ATA hardware connection can be made by linking a standard, 40-pin, ATA ribbon-cable connector from the Fast ATA drive to the local-bus host adapter. Once connected, the capabilities of Fast ATA drives usually can be enabled through the data-transfer options found in the BIOS setup tables. For further simplification, future BIOS releases should offer an automatic configuration for Fast ATA drives.

Fast ATA isn't intended to replace SCSI in higher-end applications like file servers, minicomputers, mainframes, and technical workstations. In addition to their high data-transfer rates, these platforms generally are required to handle large numbers of simultaneous I/O events from multiple users. The more highly sophisticated command-processing capabilities offered by typical SCSI devices, such as tagged command queuing and command coalescing, are better suited to these platforms. SCSI implementations also are more attractive to users that need a large number of devices (scanners, plotters, and disk, tape, and CD-ROM drives, for example) connected to their system. The added cost of a SCSI host adapter can be amortized over the large number of devices.

Contact Seagate Technology at (408) 438-6550.

RICHARD NASS

A COMPARISON OF DEVICE INTERFACES

Interface	Typical implementation	Burst-transfer rate (Mbytes/s)	Connection
Standard AT (ATA or IDE)	BIOS	4.0-8.3	ISA or motherboard
Fast ATA	BIOS	13.3	PCI, VL-Bus, or motherboard
SCSI	Host adapter	5.0	ISA
Fast SCSI	Host adapter	10.0	VL-Bus, PCI, or EISA
Fast and wide SCSI	Host adapter	20.0	VL-Bus, PCI, or EISA

DISK-DRIVE READ-CHANNEL IC MAXIMIZES PRML ADVANTAGES With "BOTTOM-UP" DESIGN

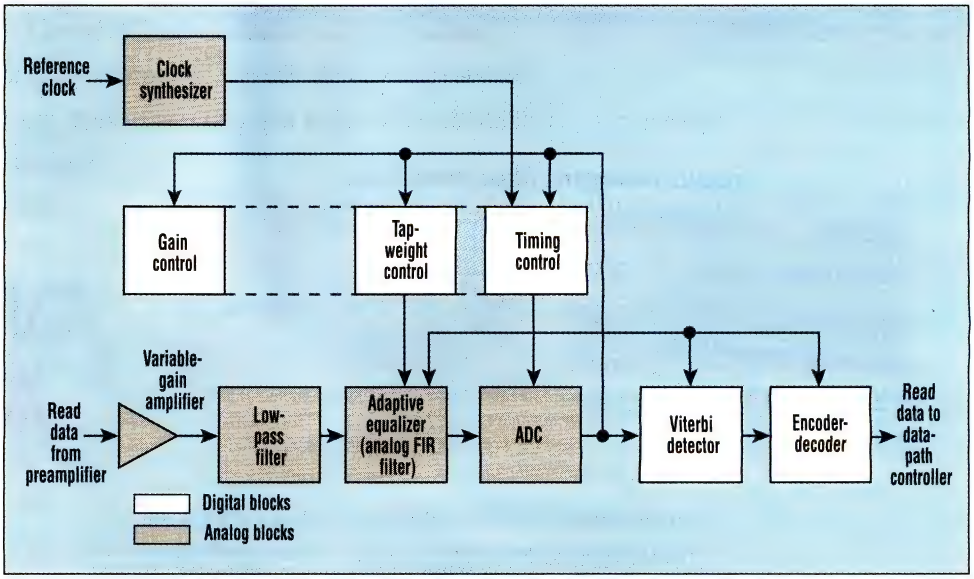
The partial-response, maximum-likelihood (PRML) signal-processing algorithm is finding its way into more and more high-end, hard-disk drives. Using PRML, engineers can replace most of a hard-disk drive's analog read-channel electronics with digital circuitry and just about double the disk's storage capacity.

With that in mind, engineers at the Mass Storage Products Division of AT&T Microelectronics, Allentown, Pa., have gone one step further. They've taken full advantage of the benefits offered by the up-and-coming read-channel technology by designing a PRML read-channel IC from the bottom up.

Emphasis was put on the design of ten-tap analog finite-impulse-response (FIR) filters. The filter implements the tap weight control in the digital domain and the tap-value summation in the analog domain. By using the analog FIR filters in place of a conventional digital FIR filter, a smaller, lower-power flash analog-to-digital converter can be employed.

The data-path performance was modeled by AT&T's designers using proprietary simulation tools. This technique allowed them to evaluate different circuit options, such as the number of taps in the FIR filter.

About 150 mW of power is consumed by the FIR filter and flash converter when the chip runs at full speed. Competitive archi-



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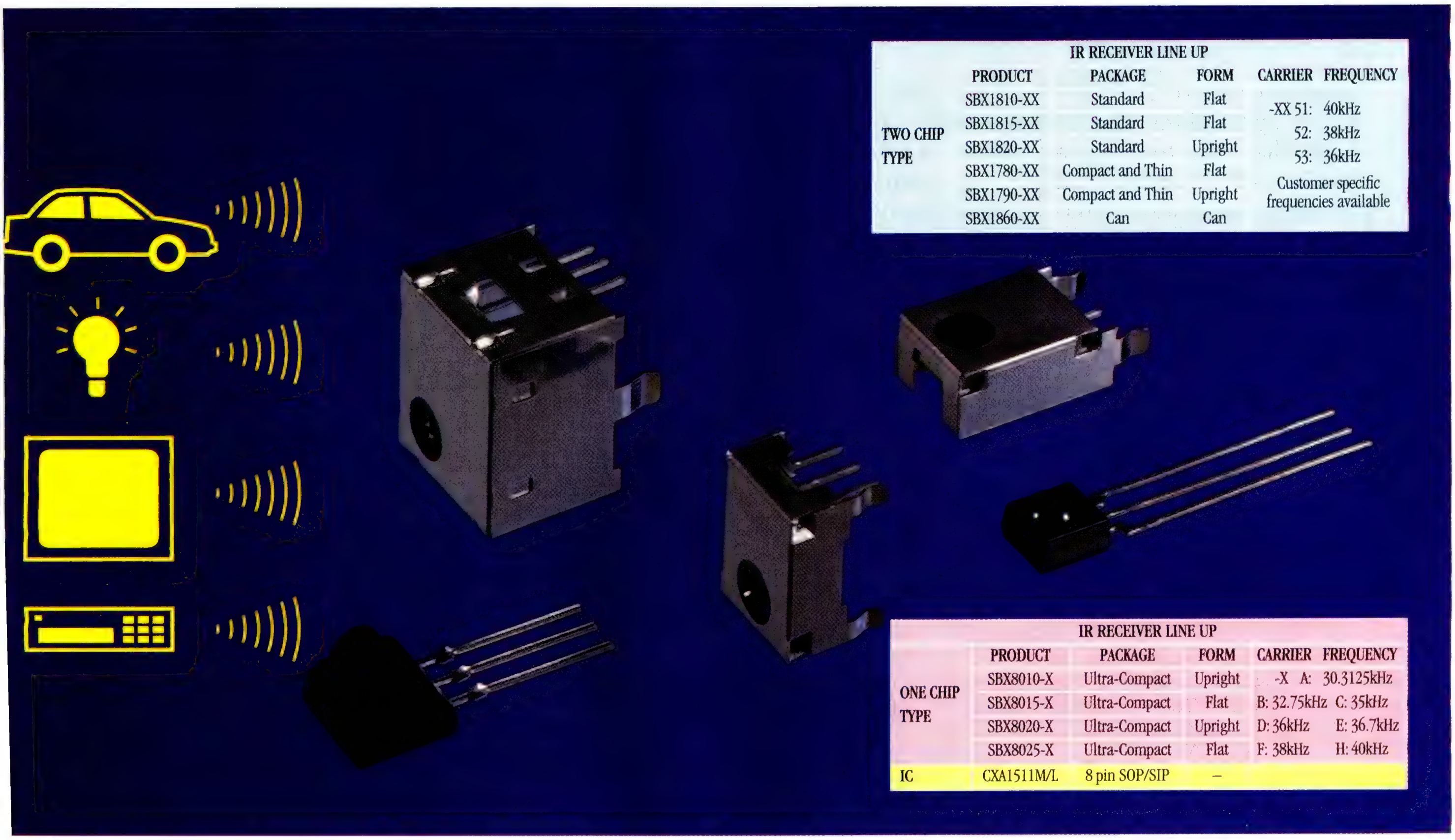

IR RECEIVER LINE UP

	PRODUCT	PACKAGE	FORM	CARRIER FREQUENCY
TWO CHIP TYPE	SBX1810-XX	Standard	Flat	-XX 51: 40kHz
	SBX1815-XX	Standard	Flat	52: 38kHz
	SBX1820-XX	Standard	Upright	53: 36kHz
	SBX1780-XX	Compact and Thin	Flat	Customer specific frequencies available
	SBX1790-XX	Compact and Thin	Upright	
	SBX1860-XX	Can	Can	

IR RECEIVER LINE UP

	PRODUCT	PACKAGE	FORM	CARRIER FREQUENCY
ONE CHIP TYPE	SBX8010-X	Ultra-Compact	Upright	-X A: 30.3125kHz
	SBX8015-X	Ultra-Compact	Flat	B: 32.75kHz C: 35kHz
	SBX8020-X	Ultra-Compact	Upright	D: 36kHz E: 36.7kHz
	SBX8025-X	Ultra-Compact	Flat	F: 38kHz H: 40kHz
IC	CXA1511M/L	8 pin SOP/SIP	–	

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READER SERVICE 133

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tectures consume approximately 600 mW. The filter requires several multipliers, multiple 6- to 10-bit-wide adder circuits, and pipelined latches. The analog functions of the read-channel chip include a variable-gain amplifier (VGA), a low-pass filter, a clock synthesizer, the FIR filter, and the analog-to-digital converter. The digital blocks include a Viterbi detector, an encoder-decoder, as well as controls for gain, tap weight, and timing *(see the figure)*.

Placing the converter after the filter in the dataflow sequence means the conversion noise isn't amplified by the filter. This allows the chip to have a smaller converter with half as many comparators. Consequently, the die size of the chip is reduced by almost 50%.

The chip's VGA gain is digitally controlled and continuously adapted when it reads data. This delivers the control required by a sampled-amplitude system. A Butterworth filter is then used as the low-pass filter because of its steep cutoff-frequency characteristic. The analog FIR filter follows and compensates for the larger group-delay dispersion, which is a characteristic of the Butterworth filter.

Because the FIR filter bandlimits high-frequency noise before analog to digital conversion, the filter's frequency-cutoff characteristic is a key parameter in a sampled-amplitude read-channel chip. At very high frequencies, there's very little signal energy. However, noise that's present must be eliminated before sampling. Otherwise the noise is aliased to the baseband, where it's nearly impossible to separate from the signal.

For tap-weight control, the AT&T engineers designed a computational unit that updates the FIR filter's tap weights using a standard DSP algorithm. The same circuit sequentially updates each tap weight while the chip is reading data, supplying a continuous adaptation and improved performance. This occurs without any external CPU intervention. The continuous adaptation offers compensation for chip-processing variations and any changes that occur during drive operation due to changes caused by temperature variation or component aging.

The chip's digital phase-locked loop (PLL) compensates for the added latency that's created by the FIR filter and the analog-to-digital converter. A digital implementation allows the PLL to synchronize more quickly to the input data stream. This results in smaller PLL sync fields.

Margin in the PRML channel, which determines whether the error budget calculated is sufficient, is measured by tracking the pulse-qualification threshold. The threshold varies until pulses drop in or out. Timing margin is also tested by offsetting the recovery window to see how much jitter can be tolerated without pushing the driver-

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error rate to an unacceptable level.

The Viterbi detector is a digital circuit that implements the architecture's maximum-likelihood portion. The detector, which operates on sequences of bits rather than single pulses, effectively replaces the symbol-by-symbol pulse-peak detector circuit that's typically employed in a peak-detect channel.

The chip's encoder-decoder circuitry, built with a scrambler, descrambler, precoder and unprecoder, and enhanced redundant address mark, increases the amount of data that can be stored on the disk. Block encode and decode functions translate non-return-to-zero data from the data-path controller into RLL (run-length-limited) modulation code. The scrambler, which comes before the block encoder, "whitens" the data's spectrum of power spectral density. Strongly colored data could cause the FIR filter to adapt incorrectly. The descrambler follows the block decoder and supplies the complementary function on the data that's read from the media.

A precode block is added to the data path after the block encoder to ensure that the run-length constraint applied by the block encoder appears at the FIR filter output. Lastly, precompensation helps modulate the timing to compensate for serious nonlinear effects that can be modeled for bit shift. This shifts write data in the opposite direction when compared to a peak-detecting channel.

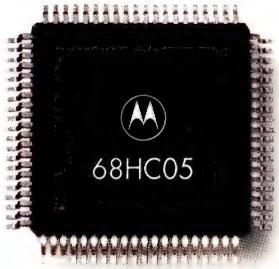
For more information, contact AT&T's Pat Mallon at (908) 771-2788 or Richard Muldoon at (908) 771-2825.

RICHARD NASS

IC PLACE-AND-ROUTE METHODOLOGY BALANCES TIMING AND DIE-SIZE TRADE-OFFS

As ICs migrate toward half-micron technology, interconnect delay dominates gate delay and largely determines chip performance. Physical layout is one of the most important steps in tackling IC-performance issues such as clock skew and crosstalk effects. That's because placement and routing determine interconnect topology and final connections, and thus associated interconnect delays.

Engineers must attack the problem with timing-driven physical design. But a difficult part of performing timing-driven design is bridging the gap between the path-oriented timing analysis in the front end of the process and the net-oriented physical design in the back end. Conventional approaches to physical IC design may be based on either net- or path-constraint



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Microcontrollers

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methodologies.

A new approach from ArcSys Inc., Sunnyvale, Calif., uses Slack Graphs for timing-constraint representation (basically, slack is the amount of excessive timing resource). The Slack Graph bridges the gap between path-oriented timing verification and net-oriented placement and routing. In actuality, it acts as a generic interface between timing verification and physical design, and is nothing more than a snapshot of the timing-verification results.

For a given design net list, the ArcSys tools form a directed graph in which each node represents a pin, and each direction edge represents the electrical connection from a source pin to a receiving pin. After delay calculation, the system then binds the intrinsic delay or RC delay (transition plus interconnect delays) to the internal cell edge and free net edge, respectively.

With specified setup-and-hold-time rules for flip-flops, latches, target clock-cycle time, external data-arrival time at primary inputs, and required arrival time at primary outputs, the Slack-Graph-based system can perform timing verification that determines actual and required arrival times at each node. Then, nodal slack of node i is defined as the difference between required and actual arrival times. The edge slack of edge (i,j) is the difference of the required arrival time at node j and the sum of the arrival time at node i and edge RC delay. Then, with the information, the system constructs a complete Slack Graph. This description is a simplified version of Slack Graph processing; in practice, it can be more elaborate.

One major benefit derived from the Slack Graph is that it serves as a generic timing interface. The graph's construction is independent of the timing model and timing verifier used. Each Slack Graph considers all timing paths. Unlike conventional approaches, though, the timing-driven design methodology using Slack Graphs can handle such practical concerns as pin-to-pin RC delay, loading effects, and slew rates.

Because the graph contains complete timing information, engineers can retrieve commonly-used path constraints from the Slack Graph. And the graph contains this information in a relatively small amount of space. Actually, its size is proportional to the number of pins in the IC design.

Slack Graphs enable the ArcSys system to simultaneously optimize die-size and all-path timing constraints when doing physical placement and routing. That's because Slack Graphs contain not only timing information, but also connectivity used for layout. The graph edge is derived from the chip's net list, and it tells exactly which pins are connected.

Because the graph can contain both types of information, ArcSys was able to develop a patent-pending optimization process that globally considers slack, sensitivity, and connectiv-

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ity. It respects existing layout results, and suggests a better timing solution. The new layout result is then fed back to construct a new set of slack numbers on the same graph. Thus, the Slack Graph optimizer and layout optimizer alternately guide the global optimization process. This allows the best tradeoff among timing and layout.

The complete ArcSys physical-IC-design system consists of seven major components: input data, parasitic extraction, delay calculation, timing verification, placement and routing, timing report, and data export.

The flexibility afforded by the Slack Graph generic timing interface lets users construct an appropriate design flow for their requirements. For example, an integrated timing-driven setup will automatically perform timing optimization. Users need only provide a timing library that includes gate delay, driving resistance, and other parameters for each cell. After users specify the target cycle time, and the actual and required arrival times for I/O pads, the ArcSys Timing Verifier locates registers and clock networks, performs timing analysis, and generates a Slack Graph for timing-driven optimization. On the other hand, a setup configured for total user control requires that users have their own timing verifier and delay calculator. Only the basic parasitic parameters, such as per-unit capacitance, are needed.

For more information, call (408) 738-8881.

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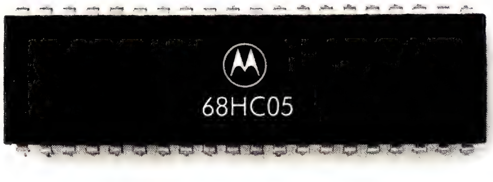

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Microcontrollers

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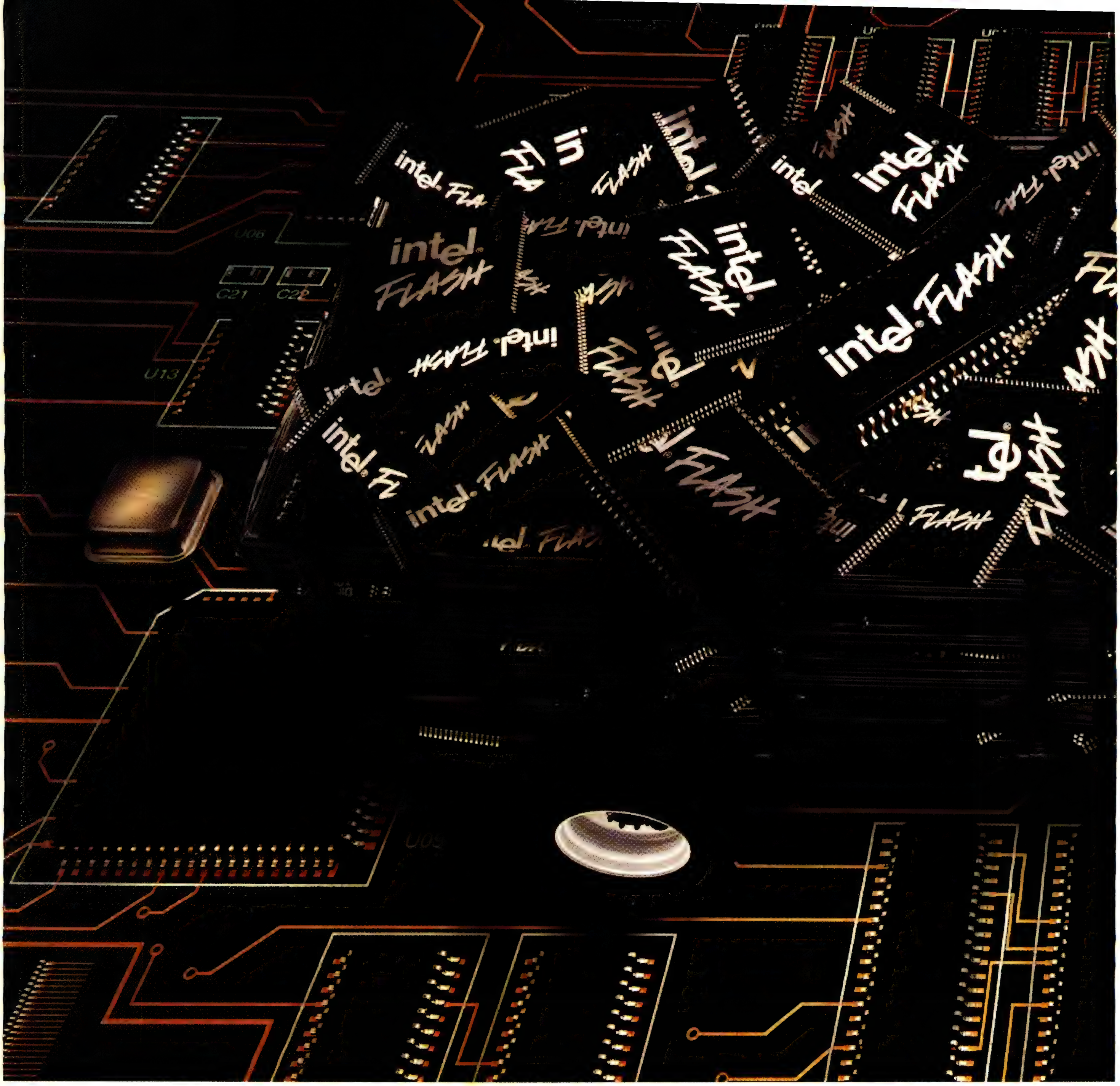

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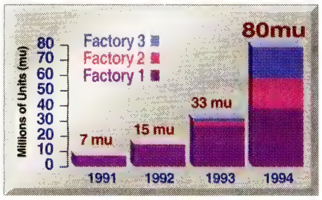
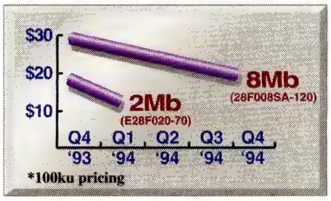


Intel Flash Component Pricing Trend*



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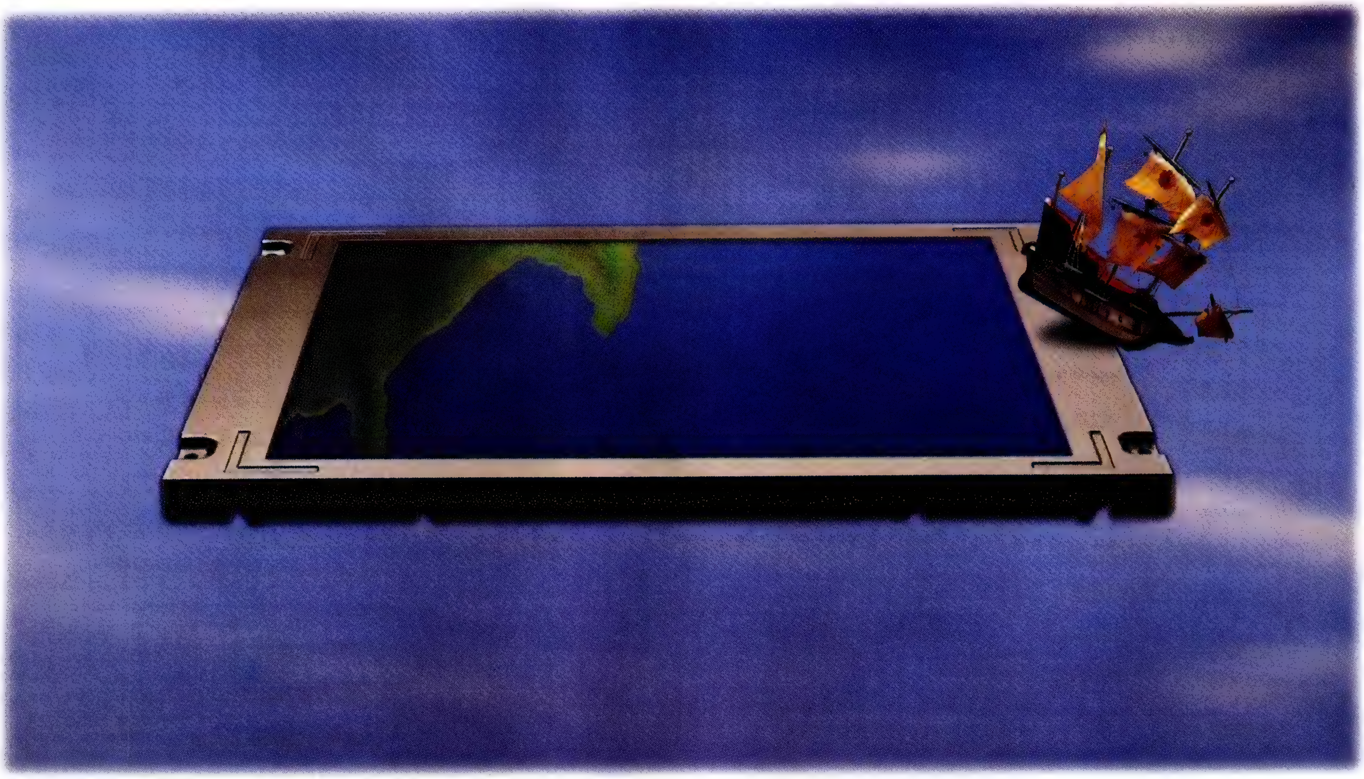

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COVER FEATURE

WITH WORD WIDTHS OF 4 TO 32 BITS, CORE-BASED DESIGNS ENSURE OPTIMIZATION.

MICROCONTROLLER DESIGN EXPLOITS REUSABLE CORES

DAVE BURSKY

As customer demands perpetually change throughout the electronics marketplace, the window of product viability continues to shrink. Feeling the brunt of this unstable climate are the designers, who are increasingly pressured to bring products to market quickly. Delivering just *one* product is no longer suitable, though, because customers often want a range of products with different features to match their needs. Not surprisingly, this same principle trickles down to the design level—designers need a range of choices to better optimize the system they're creating.

To give systems the flexibility they need, most designers have already based their systems around programmable microcontrollers or embedded microprocessors. But working with off-the-shelf microcontrollers has some limitations. For instance, they may not have enough memory, or they may not have the right mix of features. Also, some MCUs may be too feature-rich, making them too costly. Similar issues are faced by the controller-chip manufacturers, as well as by manufacturers of chips like digital-signal processors, where "spin-off" versions are desired.

To solve most of these issues, microcontroller, DSP, gate-array, and standard-cell chip suppliers, and system designers, are adopting the same approach: They're all basing most new chip designs on some form of core-based microcontroller/microprocessor to reuse previous design investments.

By breaking down a complex microcontroller or microprocessor into its basic sections—a CPU, some RAM, some ROM, EPROM or EEPROM, and various I/O functions—designers can reuse pieces of designs to quickly develop versions of chips targeted for specific applications. This rapid creation of custom solutions is being helped along by continuing improvements in design and simulation tools, the availability of megacell libraries, and the design of key circuit building blocks with reuse in mind.

The idea of design reuse isn't entirely new. The earliest microcontrollers and bit-slice processors in the late 1970s and early 1980s (such as the TMS-1000 and COPS 4 MCUs, as well as the 2900-family of bit slices) took advantage of design reuse. Companies offering 4-bit MCU families typically had several members of a series all sharing a common CPU, but each version had different support functions included. A handful of application-specific IC (ASIC) suppliers created gate-array masterslices using the 2900 series of bit slices. These masterslices had four of the 4-bit 2901 cores embedded in the array to form a 16-bit processor. Blocks of RAM and/or ROM were included to hold the microcode.

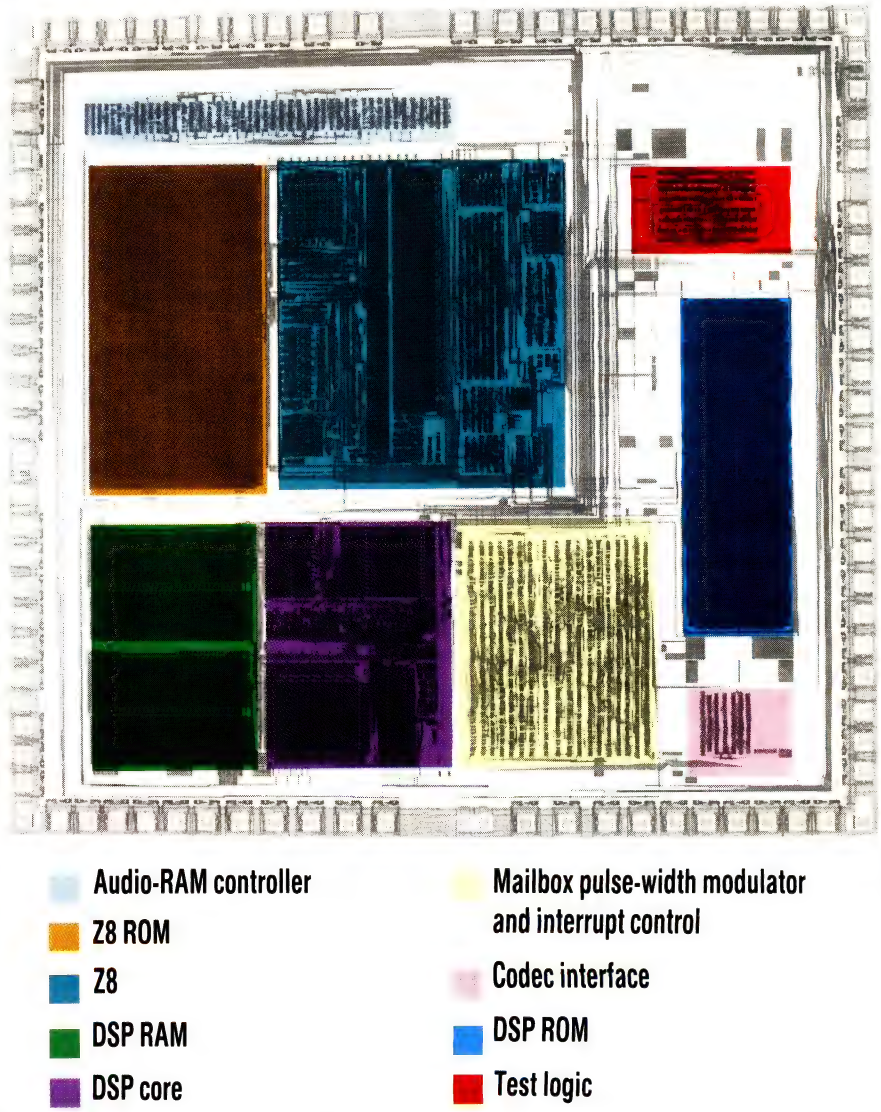
To successfully design a block for reuse, certain factors must be considered. For instance, features that let the blocks be tied together must be included. Furthermore, the design should be developed in a process that's common to the other blocks (not the case several years ago, because the process used for gate-array and standard-cell fabrication was often different from the process optimized for the mass-manufacture of MCUs). Once these two basic elements come together, along with the proper design tools, customer-specific versions of a chip can be defined and fabricated in as little as two or three months (six to nine months for a typical complex design).

When suppliers want to develop a spin-off version of one of their MCUs, they typically follow one of two major approaches, each resulting in customer/application-specific versions. In one approach, which most major suppliers of microcontrollers have used, fairly broad standard families of microcontrollers are defined—chips that the suppliers themselves proliferate.

Often, manufacturers define each chip's feature set by discussing needs with customers or surveying a particular class of applications. Then, if a supplier feels the needs are broad enough, it will develop an offshoot product. Such an approach is well established, as seen by the many successful microcontroller families available from over two dozen suppliers. For instance, there are over a dozen or more members in Motorola's 68HC05 8-bit MCU series, over a half-dozen 32-bit members of Intel's i960 RISC controller family, at least 12 members in the Philips 80C51-based family, and so on.

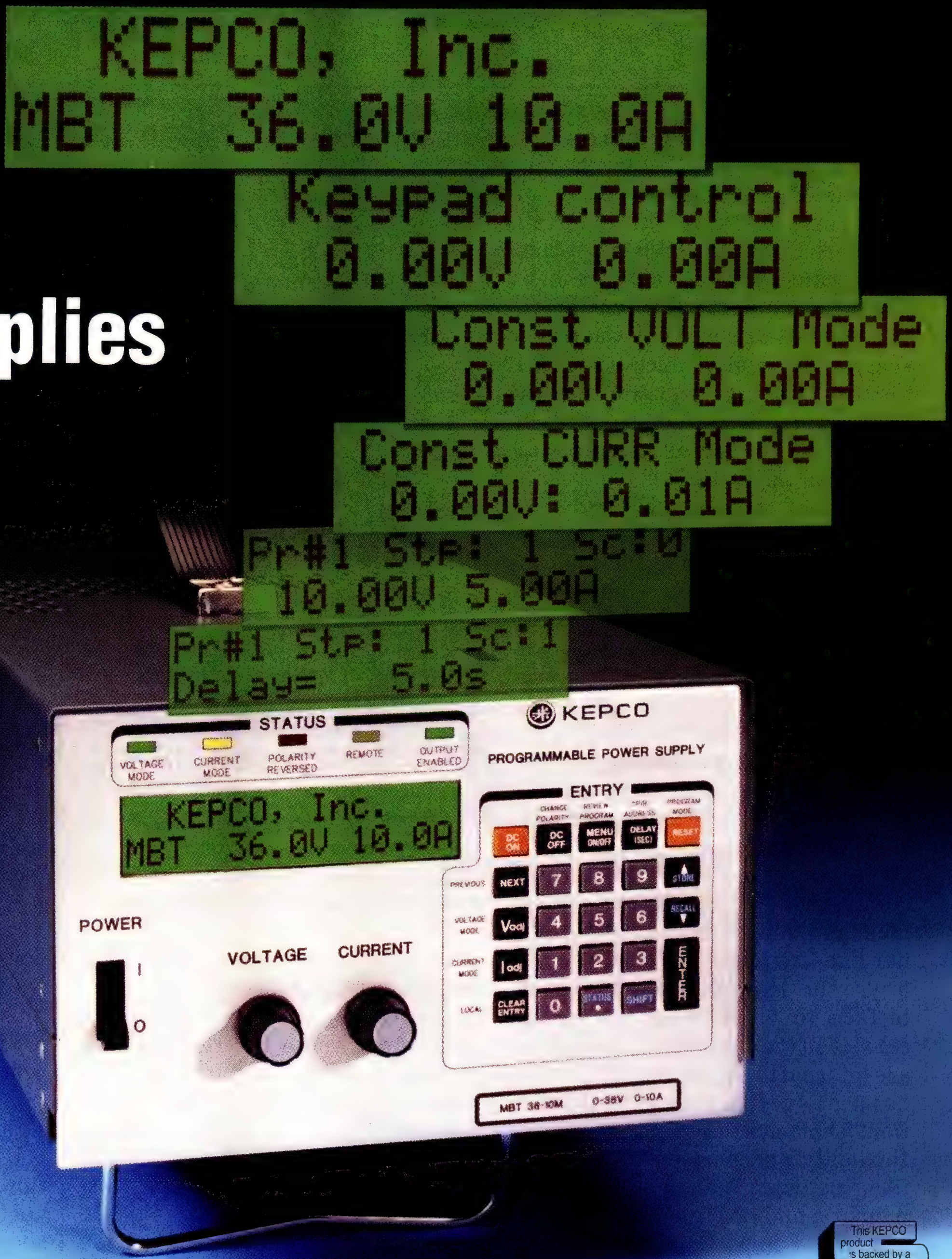
The alternative approach is to have one or more customers totally define the microcontroller's feature set. Motorola took that route in its 68HC05 8-bit microcontroller family as well, using a somewhat formalized product-definition scheme. Instead of just surveying customers, the company distributed a simple software questionnaire on a floppy disk to potential customers. The questionnaire gives these customers the opportunity to define the MCU feature set they would like.

Completed questionnaires are then collated to see if enough commonality exists for Motorola to come out with a "standard" device, which means it could be sold to more than one customer. Such an approach lowers the cost to the customer because Motorola can mass-produce one de-



1. SUPER INTEGRATION is exemplified in this chip, which combines Zilog's handcrafted Z8 microcontroller and associated ROM (upper left corner), a 16-bit DSP block and its associated RAM (lower left portion of the chip), and some custom logic (lower right and right edge of the chip) to form a single-chip telephone answering machine. The custom logic includes the test logic, DSP ROM, codec interface, mailbox pulse-width modulator, and interrupt control. Also in the upper left corner is a group of cells for the audio-RAM controller. By taking standard blocks and combining them with application-targeted support logic, designers can quickly bring custom chips to market.

Kepco power supplies talk...



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MBT MODEL TABLE

MODEL	OUTPUT VOLTAGE Volts	OUTPUT CURRENT Amperes
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MBT 15-20MG	0-15	0-20
MBT 25-14MG	0-25	0-14
MBT 36-10MG	0-36	0-10
MBT 55-7MG	0-55	0-7
MBT 75-5MG	0-75	0-5
MBT 100-3.6MG	0-100	0-3.6
MBT 150-2.4MG	0-150	0-2.4

A single board computer is included in models with suffix "G". This enables the RS 232 & GPIB (IEEE 488.2) ports and allows an MBT to act as a "master" driving other power supplies. Models are available without the G for use as "slave" units and stand-alone service. To include the Output Enable and Polarity Reversal relays, add a suffix "R" to the model number.

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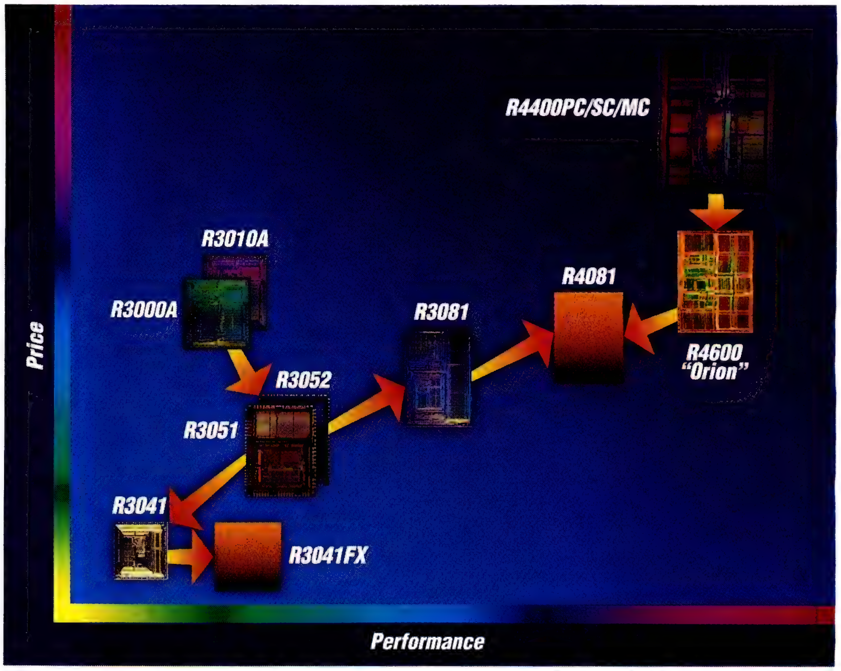
sign to satisfy several companies' needs, thus minimizing chip cost.

If the design isn't shared, the one customer that wants it would have to pay non-recurring engineering (NRE) charges and higher per-chip fees because the chip would be manufactured only for that customer. The benefit, of course, is the exclusivity of the custom microcontroller for that customer. In turn, the customer hopefully has some degree of uniqueness for the its end product. Moreover, an obstacle is placed into the path of any company trying to duplicate the system features. A compromise solution is for the customer to have a limited-time exclusivity arrangement. For example, the customer would have access to the chip exclusively for, say, six months before the manufacturer sells it as a "catalog" product.

The processor core to be incorporated on a customer-defined chip must have several characteristics, some obvious, others subtle. For instance, the core should be software-compatible with existing family members and contain all of the signal lines required by a standalone processor. However, because the interface to other functions (megacells) is on the chip, extra signals that are internal to the processor core can be used as part of the core-cell definition. That gives the designers more flexibility and permits tighter coupling between the chip's processor, memory, and I/O functions.

Another important aspect in the design of custom chips is the problem of testing those chips once it's integrated. Many different test schemes can be applied, from simple serial scan approaches to complex multiplexing and control schemes. The multiplexing approaches usually allow designers to isolate and test each block on a chip as if that block were a standalone chip.

There are two popular approaches to chip testing. One is to use the cells as is and just add on-chip buses and multiplexing logic to interconnect and isolate each block, permitting test signals to reach the desired block. Or designers can modify the megafunctions and embed test signals or logic within each block. Although the latter approach requires more work to prepare each cell, testing is easier and more thorough.



2. BY CREATING A RISC-CPU-CORE-BASED FAMILY of products, Integrated Device Technology is able to offer a range of options to system designers. Starting with the R3000 core, IDT added various amounts of cache RAM and other options to give designers a choice of chips at different cost and performance levels. At the high end of the family, the next-generation R4000-based core is being prepared to provide a range of 64-bit CPU solutions.

One company that went the embedded-test route is NEC Electronics. For its ASIC program, NEC created an on-chip Macrobus and added specialized test circuits to each major megacell in NEC's cell library. Each cell has a set of test lines connected to the separate on-chip Macrobus test bus that ties all of the blocks together. NEC's designers placed the test signals on a separate bus, rather than multiplexing them onto the function's standard I/O pins. This resolved some of the conflicts that occur when the pins for the function to be tested must supply information to the function, while at the same time they do the testing.

Zilog employs an approach it calls "super integration." Customized MCUs are implemented by starting with the core building blocks in Zilog's standard chips—the Z8 MCU or a version of its Z180 enhanced Z80 core—and peripheral functions like its serial communications controller. Then those blocks, minus the pad rings, are integrated on the same chip along with various test connections. Since each block is custom-crafted to occupy minimal area and thus sell as a high-volume standard product, the overall chip area of a super-integrated processor is about the same size as standard-cell-based designs of similar complexity.

By using predesigned chip-level functions with already-written test vectors, test-development time is shortened because those vectors can be reused to test their respective blocks on the super-integration chip. Thus, the combination of short test-development time and quick chip integration gives Zilog high marks for overall quick turnaround.

In addition, because the blocks are well defined as standalone products, little time is needed to learn how to use a new function. That also reduces the development time. As a result, designers at Zilog can quickly create application-tuned microcontrollers in their Z8 and Z180 families that can satisfy several customers.

Both Sharp and Toshiba, which are licensees of Zilog's Z80 technology, also have implemented the super-integration approach. Furthermore, Toshiba has created two proprietary

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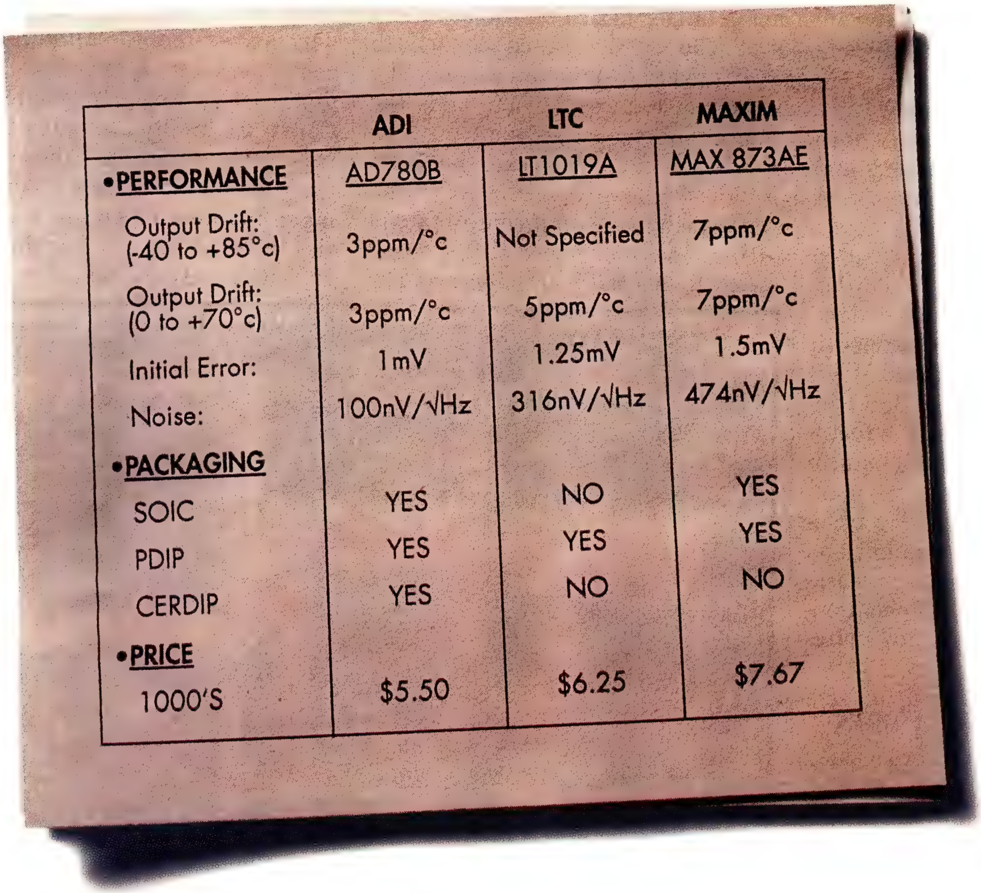

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•PERFORMANCE	AD780B	LT1019A	MAX 873AE
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Output Drift: (0 to +70°c)	3ppm/°c	5ppm/°c	7ppm/°c
Initial Error:	1mV	1.25mV	1.5mV
Noise:	100nV/√Hz	316nV/√Hz	474nV/√Hz
•PACKAGING			
SOIC	YES	NO	YES
PDIP	YES	YES	YES
CERDIP	YES	NO	NO
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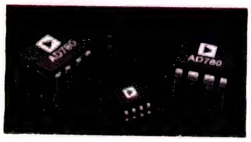

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microcontroller cores: one for high-performance 8-bit applications and the other for 16-bit system needs—the TLCS-90 and TLCS-900, respectively. The 8-bit TLCS 90 "core" is about 50% more complex than the Z80 core and runs about two to four times faster. Chips employing the TLCS 90 core can be manufactured immediately; chips based on the 16-bit TLCS 900 will not be available until late this year.

The company also added new functions to its design library, both through internal development and cross-licensing arrangements. A DSP block that was originally developed by Clarkspur, a design firm in Silicon Valley, is one such addition *(Fig. 1)*. Zilog has since enhanced the Z89320 DSP core and developed a second version capable of 20-MIPS throughputs—the Z89321. Both the older 16-bit DSP block and the forthcoming enhanced option add significant performance boosts to the main CPU when it comes to handling applications like data communications (modems), voice and image processing (multimedia), and information-storage subsystems (read/write-head positioning).

HIGH-PERFORMANCE CORES

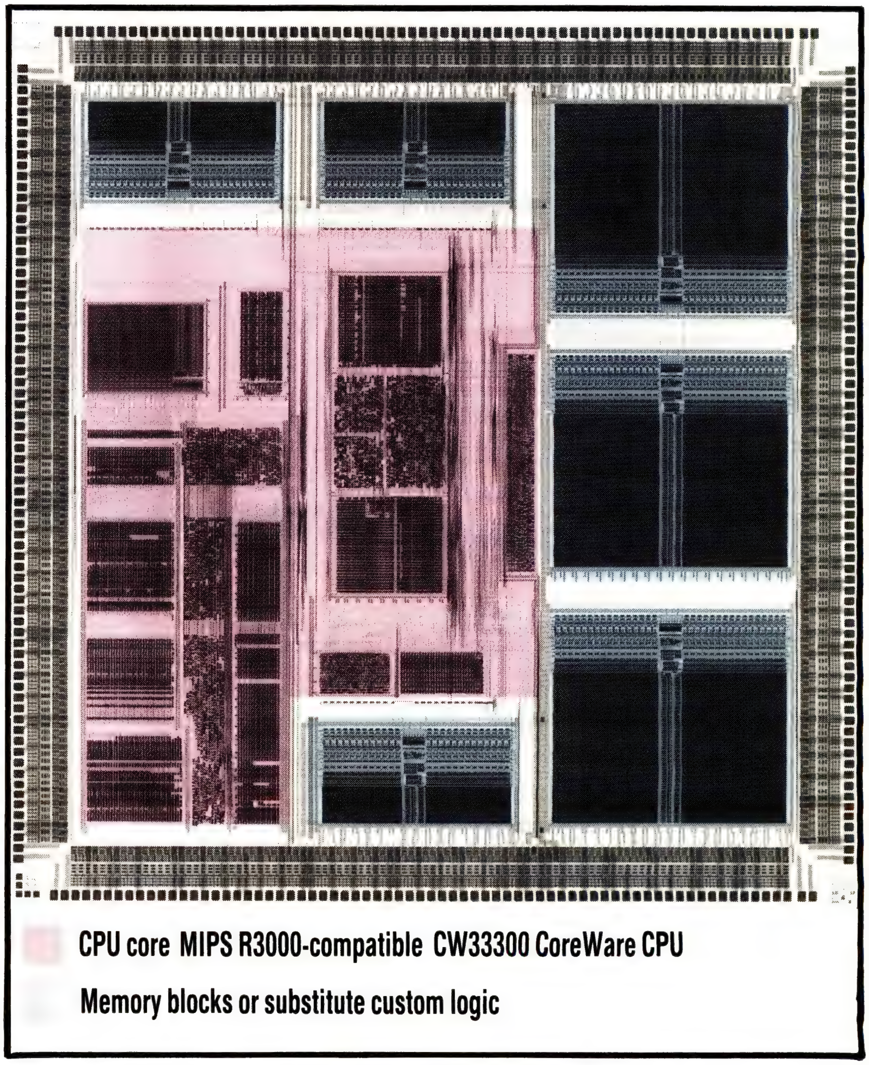
On the high end of the processing spectrum, designers at Integrated Device Technology and LSI Logic also have started with core-based processor designs based on the R3000 CPU core they licensed from the MIPS Technologies Div. of Silicon Graphics Inc., Mountain View, Calif. IDT and LSI enhanced the basic core by converting the dynamic logic to static logic, thus allowing the processor to include very-low-power standby and power-down modes.

IDT's designers have already created several spinoff versions that use the same CPU core—the R3051 and 3052 for mid-range performance, the 3041 for cost-sensitive 32-bit applications, and the 3081 for performance-critical applications *(Fig. 2)*. The main difference between the CPUs is the amount of memory included plus whether or not a floating-point coprocessor is used.

For instance, the 3041 contains a 2-kbyte instruction cache and a 512-byte data cache, while the 3051 and 3052 both pack 2 kbytes of data cache and 4 and 8 kbytes of instruction cache, respectively. All three are integer processors that deliver throughputs of 10 to 35 MIPS. An "E" extension to the architecture gives designers the option of a memory-management unit and a fully-associative, 64-entry, translation-lookaside buffer (TLB) on the 3051 and 3052. The R3081 expands the cache to 16 kbytes of instruction cache and 4 kbytes of data cache, and adds the floating-point coprocessor.

Released late last year, the 64-bit R4600 Orion processor will also serve as the seed for an entire family of higher-performance CPUs based on the R4000 MIPS architecture. The R4600 processor can deliver throughputs of up to 100 MIPS, while derivative versions, expected in late 1994 or early 1995, will provide a range of performance on either side of that number.

LSI Logic put the CPU core into the company's CoreWare design library so that customers can create their own R3000 derivatives. Such derivatives include functions like controllers for X-terminals, intelligent routers, and page printers. The CoreWare family also adds flexibility to the core design. Consequently, designers can modify the core to remove features or add new capabilities, even before placing the memory, I/O functions, or other support


■ CPU core MIPS R3000-compatible CW33300 CoreWare CPU
□ Memory blocks or substitute custom logic

3. VIRTUALLY ANY INTELLIGENT FUNCTION can be crafted by LSI Logic in its CoreWare family thanks to an enhanced R3000 CPU core. The chip shown contains the CPU core and multiple blocks of SRAM for use as instruction and data caches. Some or all of those memory blocks can be replaced with other logic functions to tune the chip for a desired application.

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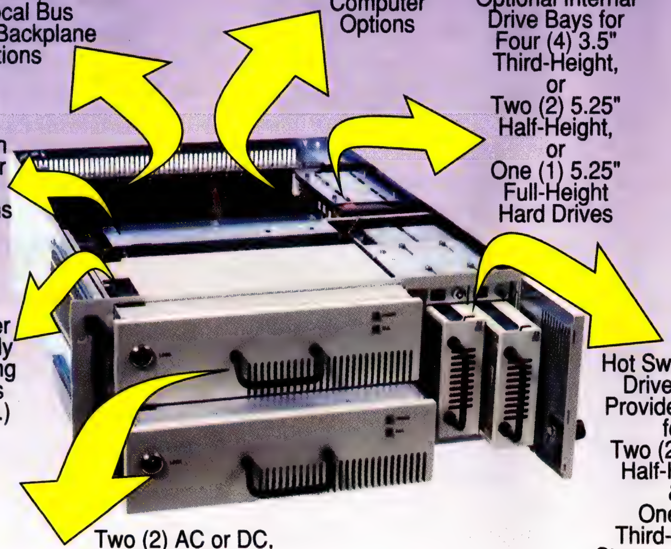
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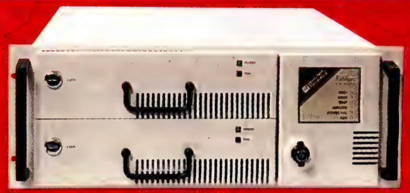
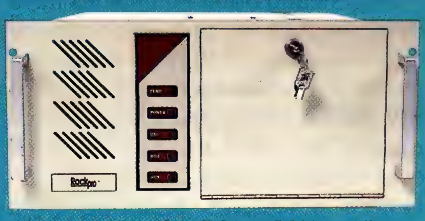
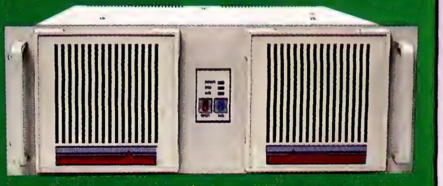


14, 16 or 18 Slot - ISA, EISA or PCI Local Bus
Fault Tolerant
FTS900

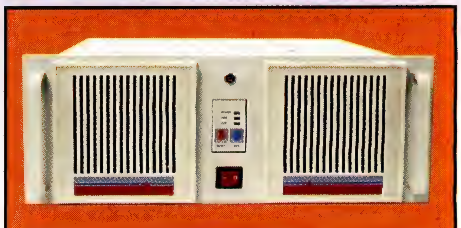


10,14,16 Slot - ISA, EISA or PCI Local Bus
CRM816

14 Slot ISA, EISA or PCI Local Bus
w/Built-In Monitor
CRM814



20 Slot ISA
CRM720



14 Slot ISA, EISA or PCI Local Bus
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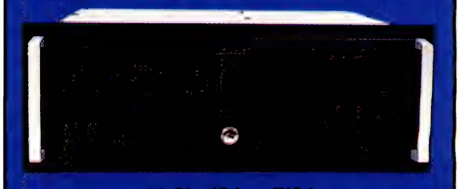

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functions around the core *(Fig. 3)*.

Other functions in the CoreWare family include blocks such as interface cells—a Fibre Channel encoder and decoder, a high-speed serial interface for gigabit/s data transfers, SCSI disk-controllers, asynchronous transfer-mode (ATM) communications networks, and so on. With these types of reusable cells, designers can create intelligent system control and interface circuits.

Fujitsu and other companies have used the SPARC processor core to create versions of the processor optimized for embedded control. The SPARClite family from Fujitsu represents the first example of such core enhancements. In addition, enhanced processors resulting from the Sun Microsystems-Fujitsu deal (to develop the microSPARC II processor) led to a much-refined process that began with the previous chip's design database. Similar activities are occurring with companies that licensed the PA-RISC architecture from Hewlett-Packard. Both Oki and Samsung are using the processor's core and then developing processors that are optimized for a range of embedded applications.

Designers at both Hitachi and NEC went in a different direction, creating malleable 32-bit RISC cores of their own. Initially targeted at applications such as personal digital assistants (PDAs), the cores can be combined with each company's ASIC design tools and libraries of megacells and logic cells.

Core flexibility also is essential for designers at S-MOS Systems. One major megacell they created is a 32-bit RISC processor that's set up as a very tightly coupled collection of smaller functions—register files, ALUs, barrel shifters, etc. Users can strip down or enhance the 32-bit RISC core, further optimizing it for cost or performance. Moreover, the RISC core can be combined with other megacells and the basic gates to craft the final design.

Taking full advantage of the modular 32-bit RISC core in its 29000 family, Advanced Micro Devices (AMD) crafted a family of processors that range in performance from the low-end 29005 to the current top-of-the-line 29050. Some differences among the family members include the absence or presence of the TLB or a floating-point coprocessor. Late last year, the company released a trio of chips—additions to the 29200

USING VHDL IN CORE-BASED DESIGNS

The VHDL modeling language is considered the worldwide standard for specifying and designing digital systems. This phenomenon is driven by the availability of software tools that use VHDL as the working input language.

Currently, several excellent simulators and logic- and test-synthesis tools make VHDL a preferred means of designing chips. This is particularly true for core-based microcontrollers and other chips that depend on reusable cores. The mixed-mode simulation capability of VHDL tools is a natural fit for core-based designs.

Mixed-mode simulation can take high-level behavioral descriptions and use them with logic-level simulations to predict the performance of a complete chip. It's this capability that eases the design of chips when it involves combining microcontroller cores with custom-designed logic.

However, core models must meet several requirements because the core is modeled behaviorally. For instance, the model should exactly match the microcontroller function and execute fast. Fast execution and compact size of the microcontroller enables designers to use cores in a full chip simulation, which also can include the designer's custom logic. With core-based simulation, users can quickly integrate board-level designs into one ASIC. The resulting ASIC reduces board space significantly. In addition, performance is typically faster thanks to the small on-chip versus off-chip interconnect delays.

The core model has two parts. The function of the core is described in pure behavioral code, while the timing is contained in a shell that surrounds the core. The timing shell has clock-to-output delays and generic parameters that serve as placeholders for back-annotated wire delays and loading effects. Input setup and hold checks are built into the shell.

By keeping the timing separate from the function, the timing parameters can be developed without a deep understanding of the core's internal function. The ASIC design also must conserve the core interface so that the core's test patterns can be used. This frees designers from worrying about the core tests, allowing them to concentrate on the rest of the logic. Test strategy for the additional logic can include a scan path that creates wide test coverage with minimal effort.

Mixed design styles are possible. Users can develop the rest of the design with either schematic-capture, behavioral modeling with synthesis, or both. Behavioral blocks can be synthesized one at a time, allowing incremental functional simulation. VHDL configurations can associate either the behavioral or structural model with the design. Users don't have to know VHDL to use models because structural VHDL can be created directly from schematics. But if designers prefer, they can first develop behavioral blocks that remain technology independent. They can thus test various implementations before committing to a gate-level design.

An emulator interface also is required. This is easily supplied because modeling in a HDL creates emulator-like functionality in a simulation environment. The model can provide disassembled instruction streams and the environment is fast enough to use the simulator fo the task of software development.

The design-for-test factor is the other crucial element in core-based chip design. One typical series—that are more highly integrated and contain resources optimized for different application areas. One such new chip, the 29245, is optimized for page printers, and even includes a high-speed video data port.

Another important factor in the RISC core is chip area. Chip cost often is directly related to the chip area. If the core is smaller, the overall chip is smaller, and that should reduce chip cost.

In one example of this trend, the ARM processor developed by Advanced RISC Machines Inc., Los Gatos, Calif., has several variations licensed by Cirrus Logic, GEC Plessey Semiconductors, Sharp Electronics, Texas Instruments, and VLSI Technology. The latest incarnation unveiled last year, the ARM 7 series, will be implemented as a core as well as in standard products. The family consists of an enhanced core that can deliver over 20 MIPS. When merged into the various cell libraries, it will make possible a wide range of high-performance embedded controllers, low-chip-count PDAs and other handheld computers.

VLSI Technology, using its ability to create large ASICs, could combine the ARM core and its FlexArray ASIC family to create sea-of-gate arrays with the RISC core prediffused in the array. Such an option would allow system designers to create custom microprocessors or microcontrollers with the short turnarounds and lower NRE charges of a gate array.

The impressive gains in 32-bit RISC processor customization also can be achieved in 32-bit CISC processors. Motorola's 68300 family is a good example of how core-based designs can proliferate. Starting with the 68000-class processor core, the microcontroller family includes several members that are targeted at a wide range of applications, including communications control, timing and motor control, and page printers.

Two of the latest chips to emerge from Motorola include the 68349—a highly-integrated 68020-class CPU, and the 68322, a 68010-class processor designed to reduce the complexity of page printers. The 68349 includes many of the features needed to reduce the complexity of a PDA—the first PDA application of the chip is in the target platform design developed by General Magic Inc., Mountain View, Calif. Along with

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method involves isolating the CPU core from the rest of the on-chip circuitry. That makes it possible to test the MCU core with the full production test used for the standard CPU. Scan paths are placed within the custom logic, permitting automatic generation of tests that have high fault coverage. Memories are also tested independently with built-in self-test circuits.

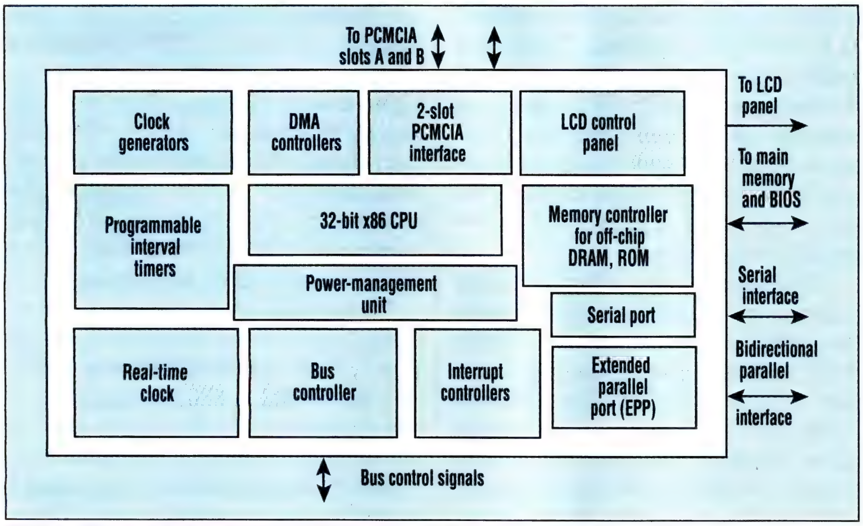
In the accompanying code example, the VHDL listing describes the operation of an I/O port on the microcontroller *(see the code listing)*. The behavioral description of an 8-bit bidirectional I/O port illustrates both the use of VHDL and the concept of separating the timing from the behavior. The first half describes the input definition logic, while the lower-half of the listing describes how the cell operates as a port output. Note that a VHDL process is a model with sequential statements that loop continuously unless held by a wait statement. Otherwise, the software code executes in zero time relative to the simulation time step.

```
--port input

read _ port : process

     read _ timing _ error : boolean := false;

     begin
          --drive internal data bus from port input data
          wait until EXT _ RD = '1';

          while EXT _ RD = '1' loop
               for  IDX in 0 to 7 loop
                    IDB(IDX) <= PORT _ PIN(IDX));
               end loop;

               read _ timing _ error <= chk _ timing(PORT _ PIN);

               wait on PORT _ PIN, EXT _ RD;
          end loop;
end process;

--port output driver

write _ port : process
    begin

    wait until EXT _ WR = '1';

    while EXT _ WR = '1' loop
         for IDX in 0 to 7 loop
              if IDB(IDX) = '0' then
                   PO(IDX) <= '0' after delay _ func(hi _ lo)
              else
                   --this output port has weak pullup (H)
                   PO(IDX) <= 'H' after delay _ func(lo _ hi);
               end if;
         end loop;
    wait on IDB, EXT _ WR;
    end loop;

end process;
```

The input process "read_port" is active when the EX_RD signal (external read) is high. When this is true, the process loops through the port bits and copies the port pin data (PORT_PIN) to the internal bus (IDB). After copying the data, the process waits for any change on the external signals or EX_RD. Correct timing is checked by calling a subroutine (chk_timing-(PORT_PIN)) to check if setup requirements and hold-time requirements are met.

The output process "write_port" is similar to the input process, except that data direction is reversed. This particular output has an open drain with pull-ups, so that the high state is a weak 'H' rather than a strong '1'. The output calls "delay_func" to add any load-dependent delay to the output transition.

Contributed by Steve McChrystal and Jim Tobias, Siemens Corp.



4. THE ELAN HIGH-INTEGRATION 386-CLASS processor developed by Advanced Micro Devices offers a base architecture and feature set that can be optimized for personal digital assistants and other portable computing platforms. All of the basic system features are on just the one chip. The optimization could take the form of removing functions to shrink chip area, or adding new functions to eliminate another chip in the system.

the CPU, the chip includes several serial ports, a memory controller, multiple timer-counters, and many other control and interface blocks. Similarly, the just-released 68322 page-printer controller includes all of the features needed to implement a high-performance but low-cost 600-dot/in. laser printer.

In the world of x86 processors, Intel has probably created one of the most prolific families of products off its 80386 and 80486 CPU cores. Between the SX, DX, the new embedded EX version, and other various options, Intel offers over a dozen chip variations. Thus far, however, Intel has resisted developing customer-specific versions, instead leaving that choice to partners and competitors.

The same reusability is the key focus of such manufacturers as VLSI, AMD, and other x86 processor suppliers, who now offer a wide range of processor options as well as the ability to create customer-specific versions. In a licensing deal with Intel to obtain the 80386 core, VLSI Technology crafted the Polar two-chip set. It will form the heart of a PDA that Compaq Computer Corp. hopes to introduce in late 1994. The initial version was defined by Compaq, but the Polar chip-set features are part of a design library that can be manipulated by a customer to tune the chip set to the customer's application.

Similarly, designers at AMD assembled the ELAN chip set, also a highly-integrated, 386-class single-chip solution that can be optimized to customer specifications *(Fig. 4)*. Various major blocks that surround the CPU core include an LCD panel controller, a PCMCIA memory-card interface port, serial and parallel ports, real-time clock, and interrupt and DMA controllers. Designers can

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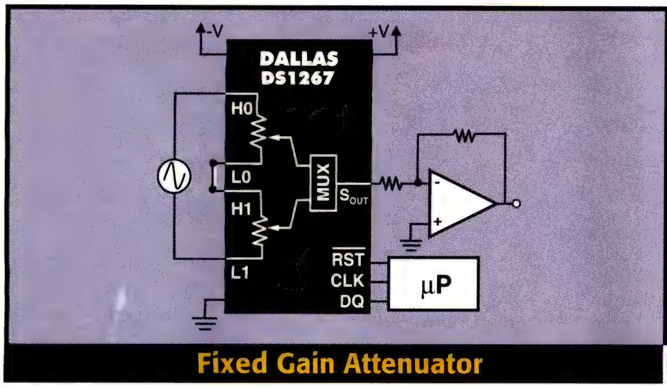
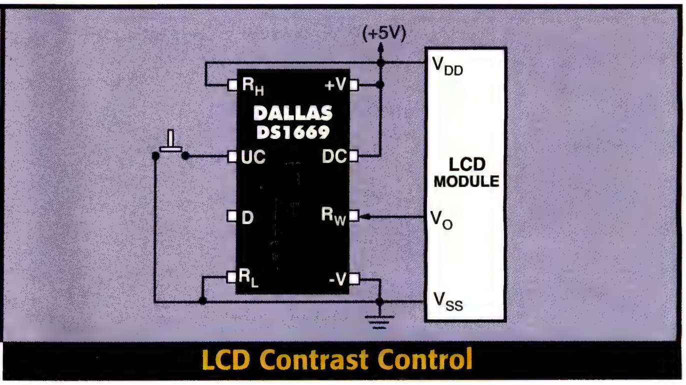
Digital Pots Simplify Adjustments



Fixed Gain Attenuator

Processor control of an analog gain stage is readily implemented using the DS1267 or DS1667.



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DS1267	2	± 5V	+5V or ± 5V	3-Wire Serial	10K, 50K, 100K	256	14-Pin DIP 16-Pin SOIC 20-Pin TSSOP
DS1666	1	± 5V	+5V or ± 5V	3-Wire Serial	10K, 50K, 100K (Log Taper)	128	14-Pin DIP 16-Pin SOIC
DS1667	2 Pots 2 Op Amps	± 5V	+5V or ± 5V	3-Wire Serial	10K, 50K, 100K	256	20-Pin DIP and SOIC
DS1668	1	8V	4.5V min 8.0V max	Single Contact Closure	10K, 50K, 100K	64	6-Pin Module w/Integrated Pushbutton
DS1669	1	8V	4.5V min 8.0V max	Dual or Single Contact Closure	10K, 50K, 100K	64	8-Pin DIP and SOIC

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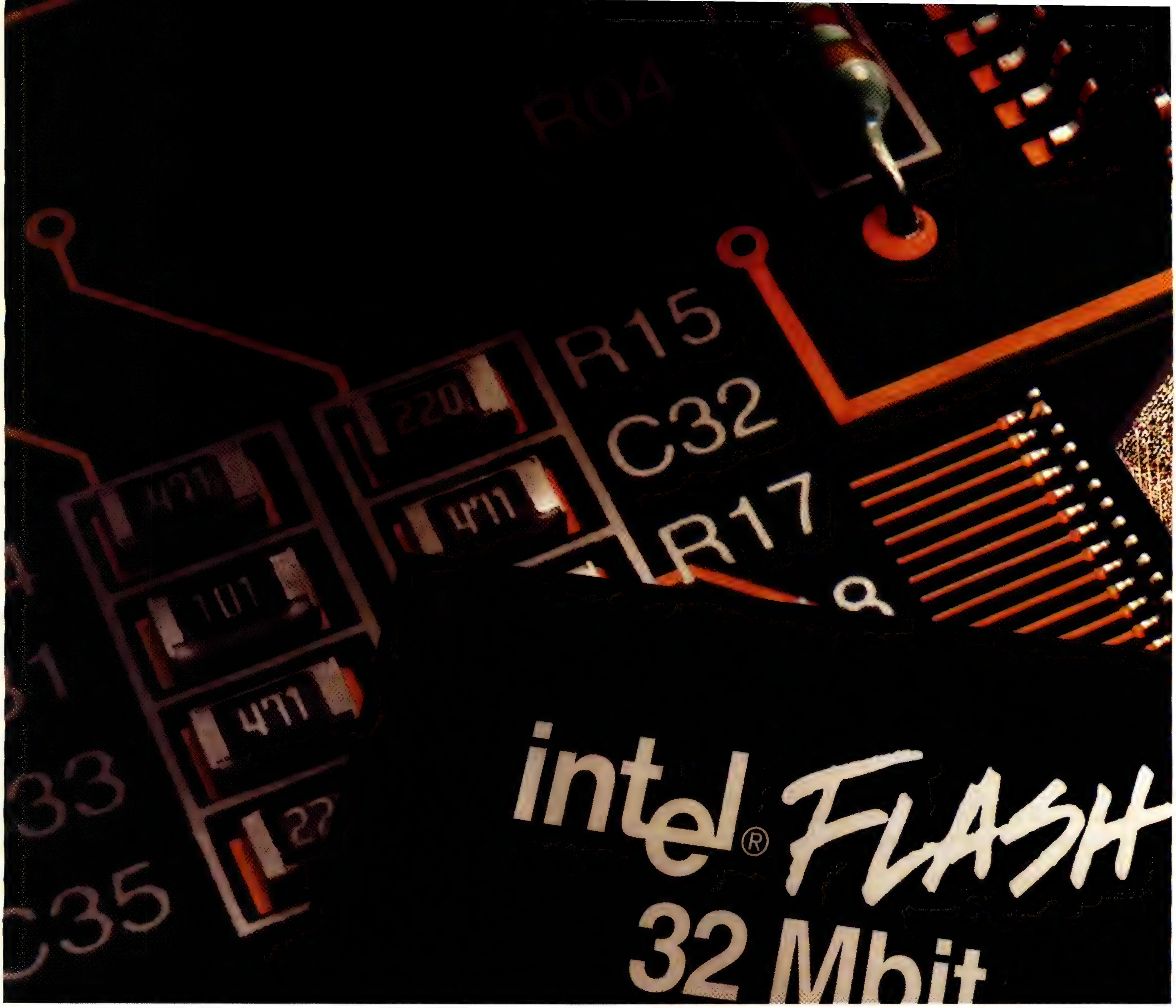

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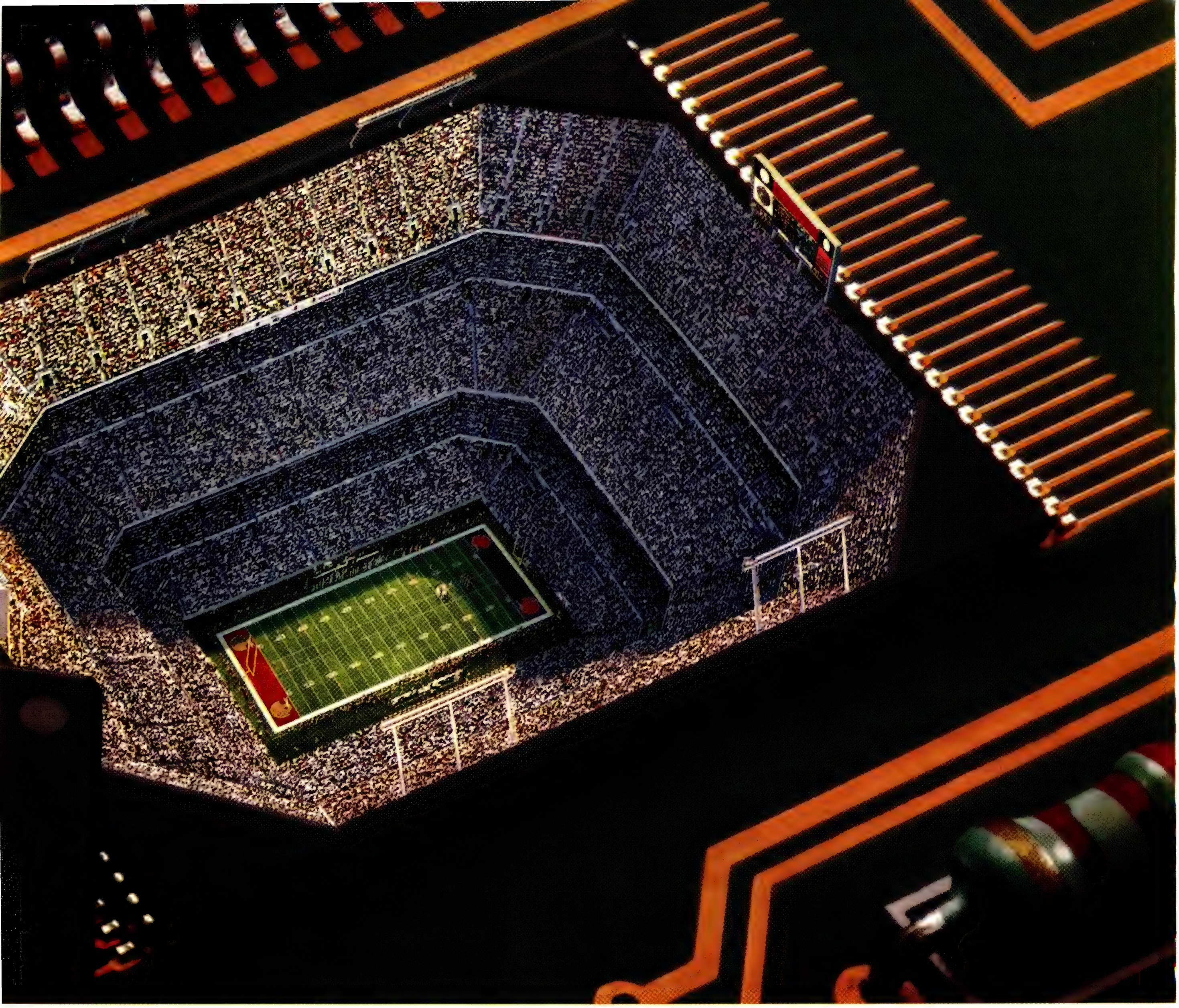

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then either remove some of these blocks or add other blocks to further optimize the chip to their application.

Although a tremendous amount of interest exists at the high end of the processor families, 16-, 8-, and even 4-bit microcontroller families also are reusing the CPU core as well as various interface blocks. The 16-bit arena has just a few offerings, almost all in the CISC world—Intel with its decade-old 80186 and 80C196 processors, Motorola with its year-old 68HC16 family, and several 16-bit MCU suppliers like Hitachi, NEC, Oki, and Toshiba. One of the few ASIC-based 16-bit RISC engines was created by Harris Semiconductor Corp., Melbourne, Fla., in the late 1980s. However, the architecture was optimized for direct execution of Forth-language instructions. It fared poorly and for the most part was withdrawn from the market (Harris does still sell it to several military customers).

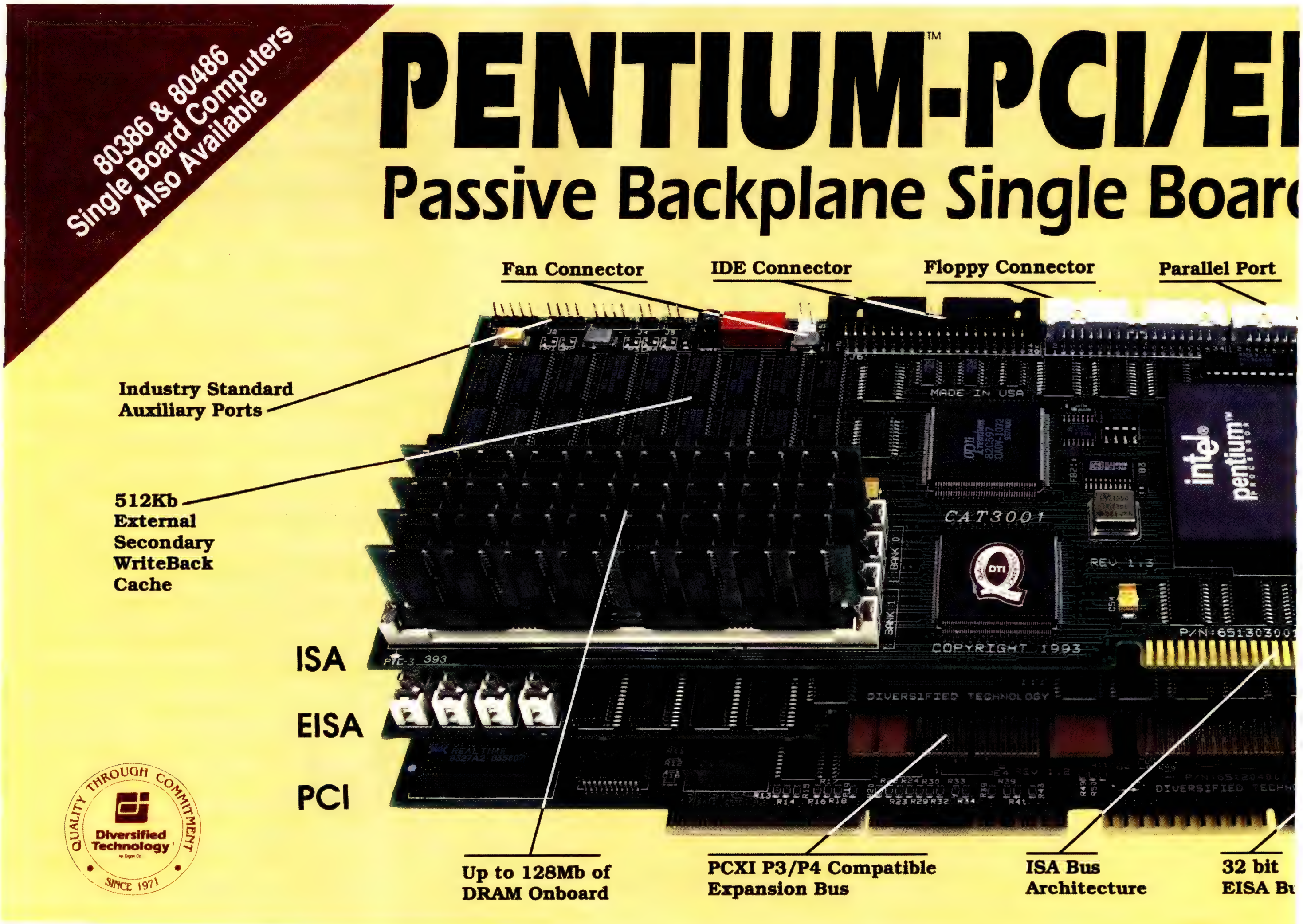
One of the latest 16-bit microcontrollers to enter the market, the Siemens SAB80C16x series of MCUs, provides a family of at least three chips, each based on the same 16-bit CPU. A recent licensing arrangement with SGS-Thomson Microelectronics further expands the family. SGS licensed the core in return for developing a version of the MCU that employs electrically reprogrammable flash-EPROM memory for the program store. Both companies will manufacture flash-EPROM versions of the chip with, initially, up to 32 kbytes of nonvolatile storage.

As with most new MCUs, the family was developed with modularity in mind—the CPU is tied into on-chip memory blocks and the basic interrupt and system control circuits. All of the modularly-designed peripherals are interconnected through an intelligent bus subsystem that uses 32-bit buses between the on-chip ROM or flash EPROM to achieve 32-bit class performance.

The CPU requires just a single 100-ns clock cycle to execute just about any of the chip's instructions, resulting in a high CPU throughput. Surrounding the 16-bit core on the "standard" versions are two serial ports, a 10-bit analog-to-digital converter (ADC), various programmable I/O lines, a 16-channel capture/compare timing block with five 16-bit counter-timers, 1- or 2-kbytes of static RAM, and up to 32 kbytes of ROM or flash EPROM.

HDLs Hasten Designs

Creating a custom version of the Siemens MCU also is quite simple. That's because Siemens employs high-level-language models with which a design can be simulated. By modeling the core and various peripheral interface functions, designers can work out most, if not all, of the design bugs before silicon is manufactured. That means working silicon can be delivered the first time around through the design cycle *(see "Using VHDL in core-based de-*



signs," p. 60).

Many other processor and ASIC suppliers also extensively use various HDLs. Besides finding design flaws before silicon is created, HDLs help reduce time-to-market since they can be linked to logic-synthesis tools and test-program-generation software. Thus, as the logic design nears completion, so does the test program and even some of the systems the chip will go into, because the simulations can often include all or part of the host system that accepts the chip.

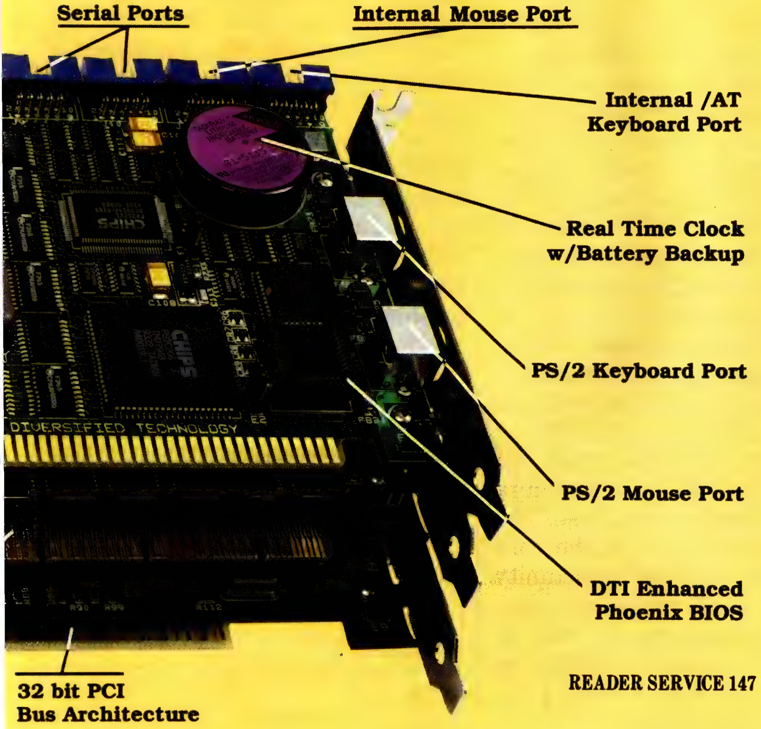
Banking on its experience in the 8-bit world, designers at Motorola moved up to 16-bit processing power with the 68HC16 microcontroller family, all using the same core CPU. There are currently six members defined in the family, with only three or four now available. Each differs in the amount of RAM, ROM, and I/O resources.

Core-processor use in the 8-bit world is probably the most prevalent, with many designs based around the Intel 8051 and all of the 8051's licensed and privately-developed offshoots (AMD, Atmel, Dallas Semiconductor, Philips, Siemens, and others). In addition to the broadly-sourced, Intel-compatible families, many other popular core-based single-sourced families exist: these include the H-8 series from Hitachi; the PIC family from Microchip; the 6805 series from Motorola; the ST-9 series from SGS-Thomson; and families from National Semiconductor, NEC, Oki, Texas Instruments, Toshiba, and as mentioned at the beginning of the article, Zilog.

Just about all of these processor families are based on a highly modular architecture that allows the chip's designers or users to define application-optimized versions. In Motorola's 68HC05 family, for instance, the core CPU is used repeatedly in conjunction with differing sets of on-chip resources.

Take, for example, Motorola's 68HC05H2, an MCU optimized for controlling high-current motor loads. The chip includes the CPU core and dual pulse-width-modulated drivers, 2 kbytes of ROM or EPROM, 128 bytes of RAM, a quadruple voltage comparator, a serial port, and the first integration of lateral-diffusion MOS transistors that implement high-current H-bridge drivers *(Fig. 5, left).* In another design, the same core is combined with 512 bytes of RAM, 12 kbytes of EPROM, a small EEPROM, a multichannel ADC, a voltage regulator, and special communication circuits needed to multiplex signals over automotive harnesses *(Fig. 5, right).*

Probably the most widely alternate-sourced family of microcontrollers, the 8051 architecture, has spawned dozens of commercially available variants as well as an untold number of custom-crafted versions sold to single customers. One of the broadest family offerings comes from Philips, which took the



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512Kb WriteBack 2nd Cache	✓		
256Kb/512Kb WriteBack 2nd Cache		✓	✓
Up to 128Mb DRAM Onboard	✓		
Up to 192Mb DRAM Onboard		✓	✓
8Kb EISA Non-Volatile RAM		✓	
FLASH BIOS Support		✓	✓
2 Serial Ports / 1 Parallel Port	✓		
IDE/Floppy Interface	✓		
PS/2 Mouse Support	✓	✓	✓
/AT-PS/2 Keyboard Support	✓	✓	✓
ISA Bus Architecture	✓		
EISA Bus Architecture - Up to 8 EISA Bus Masters		✓	
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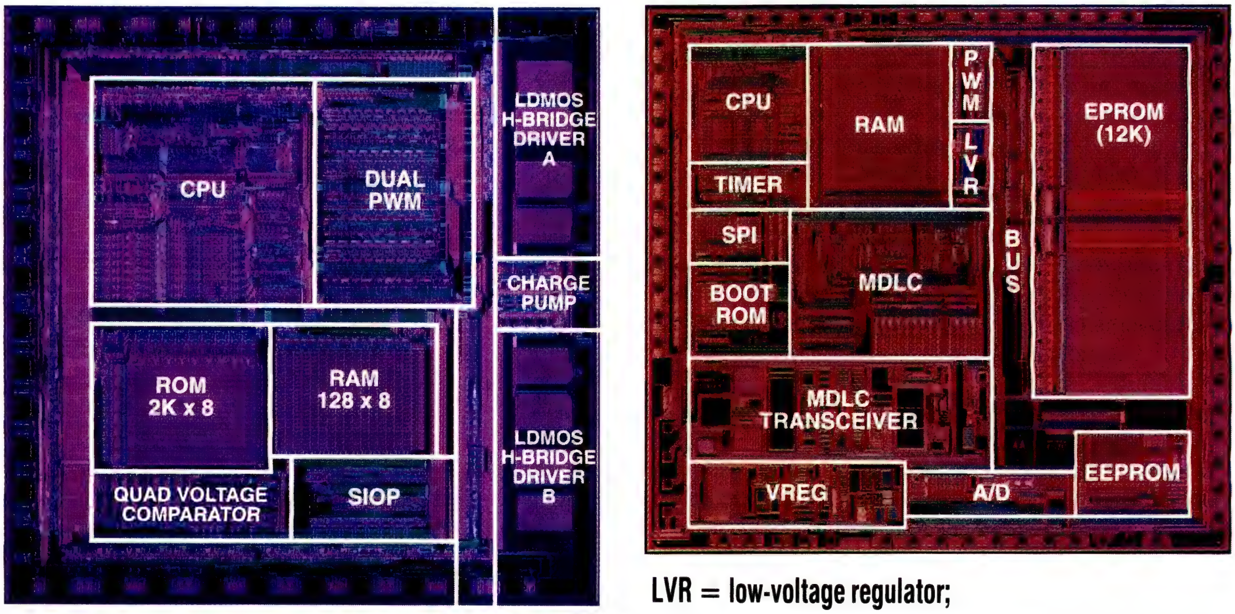

LDMOS = lateral-diffusion MOS; SIOP = serial I/O port

LVR = low-voltage regulator;
MDLC = Motorola data-link controller;
SPI = serial-to-parallel interface;
VREG = voltage regulator

5. BY REUSING THE 68HC05 CORE, designers at Motorola are able to quickly develop new system solution chips. On the left, the CPU core (upper left corner) represents the heart of a motor controller. The core is surrounded by a dual pulse-width-modulation control circuit, 2 kbytes of ROM, 128 bytes of RAM, lateral-diffused MOS power transistors for the H-bridge motor drive, and other circuits. The photo on the right is a communications circuit for automotive networks, with the 68HC05 core occupying only a small portion of the chip (upper left corner). Included are RAM, 12 kbytes of EPROM, some EEPROM, a multichannel analog-to-digital converter, the special serial communications interface, and other subsystem support.

80C51 core and developed a handcrafted, very small-area core. The core contains an internal bus optimized to allow memory blocks and other peripherals to easily be "bolted" on. All of the cells that tie into the bus are designed to meet a set of logical, electrical, and timing specifications to ensure that they can work together.

The company is currently developing an extended core megacell, the 80C51XA, which will deliver about 10 times the compiled performance of the standard 80C51 core at the same clock frequency. As with the current core-based approach, the XA version also will employ a modular architecture and a well-defined on-chip intercell bus to ease the creation of application-optimized versions. The company's extensive cell library provides a wide range of megacells as well as other building blocks—various memory blocks (RAM, ROM, EPROM, and EEPROM), a wide range of I/O port options, serial interfaces (UARTs, the inter-IC and Access.bus buses, etc.), timer-counters, ADCs, a PC/AT bus interface, and a TV on-screen display.

Not yet widely known in the U.S. is the ST9 microcontroller family from SGS-Thomson. It offers many features reminiscent of 16-bit processors—a large address space of 16 Mbytes if an on-chip MMU is used, or 128 kbytes without the MMU. The CPU core includes 224 general-purpose data registers that also can be used as 112 16-bit registers for handling multiplication results and other wide-word operations without doubling the internal bus traffic. An on-chip DMA controller gives the processor the ability to manage large data transfers with ease. The highly modular design of the core gives SGS designers the opportunity to provide a wide range of "standard" catalog versions, as well as craft application-tuned versions as the need arises.

One of the mainstays in the microcontroller area is the venerable 6502 microprocessor core. It forms the heart of many intelligent peripheral controllers in a number of the Macintosh computers from Apple Computer Inc. Available from NCR and other sources, the 8-bit engine provides designers with a small-area moderate-performance core that can be combined with the large range of cells available in NCR's standard-cell library (megacells such as SCSI controllers and communications controllers). NCR, however, also has crafted a RISC processor that its Colorado Springs division uses as an on-chip controller for a family of intelligent SCSI controllers.☐

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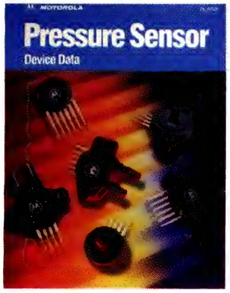

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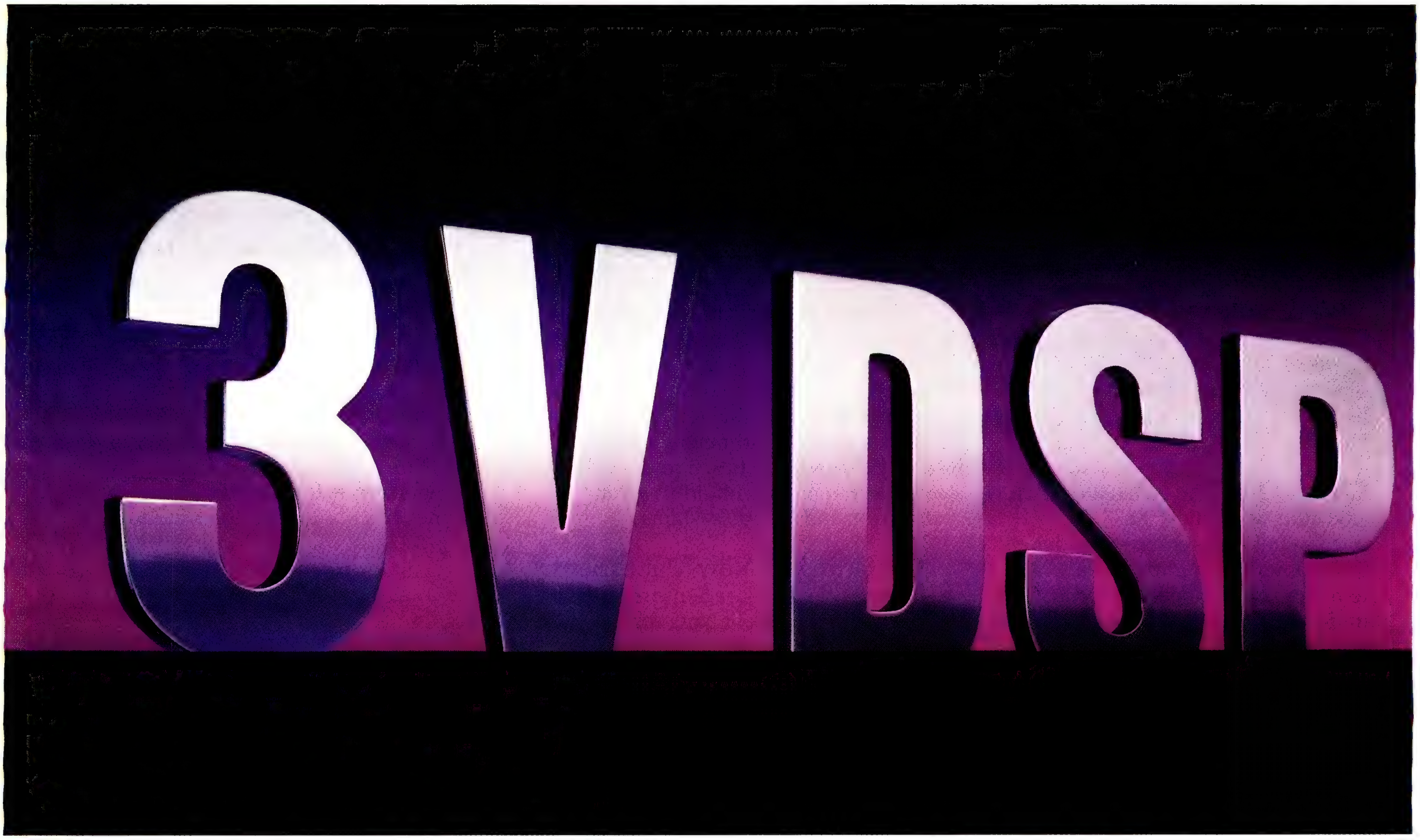

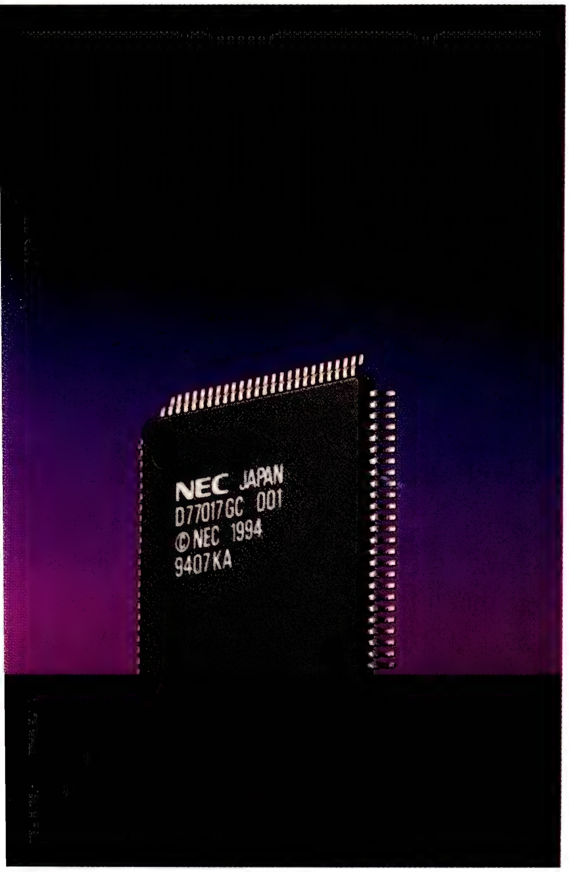

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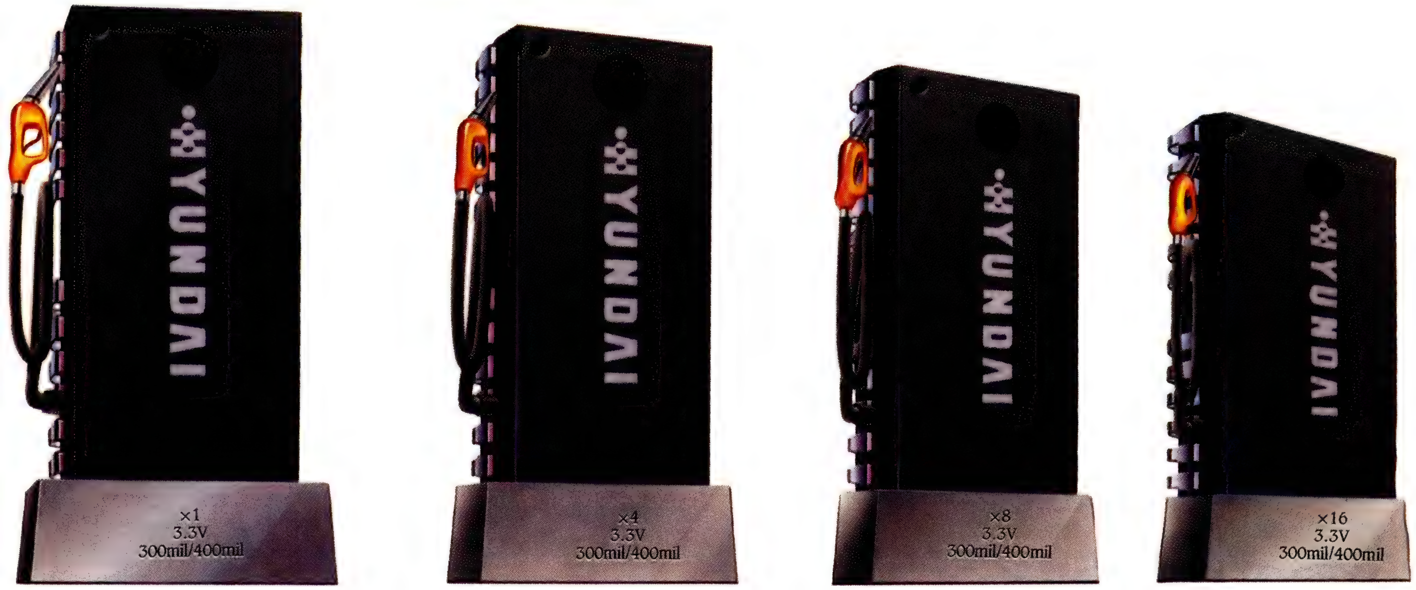

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	HY5116100A	5V	50/60/70	L, 2K/4K, SR	Q3, 94
	HY51V16100A	3.3V	60/70/80	L, 2K/4K, SR	Q3, 94
×4	HY5116400	5V	60/70/80	L, 2K/4K, WPB	Now
	HY5116400A	5V	50/60/70	L, 2K/4K, WPB, SR	Q3, 94
	HY51V16400A	3.3V	60/70/80	L, 2K/4K, WPB, SR	Q3, 94
×8	HY5116800	5V	70/80/100	L, 2K/4K, WPB	Q3, 94
	HY5116800A	5V	60/70/80	L, 2K/4K, WPB, SR, EDO	Q4, 94
	HY51V16800A	3.3V	70/80/100	L, 2K/4K, WPB, SR, EDO	Q4, 94
×16	HY5116160	5V	70/80/100	L, 1K/4K, WPB, 2C/2W	Q3, 94
	HY5116160A	5V	60/70/80	L, 1K/4K, WPB, SR, 2C/2W, EDO	Q4, 94
	HY51V16160A	3.3V	70/80/100	L, 1K/4K, WPB, SR, 2C/2W, EDO	Q4, 94

- Package: SOJ/TSOP II (standard/reverse)
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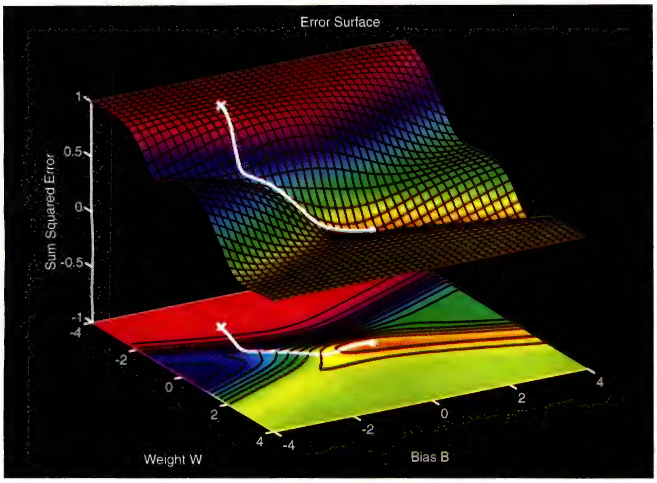

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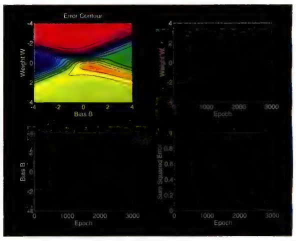

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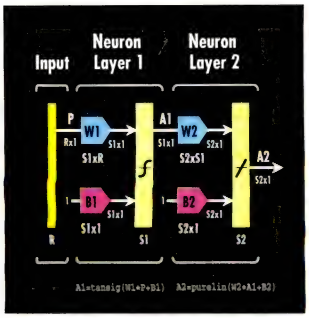

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FUZZY LOGIC IS SHEDDING ITS "HALF-BAKED" IMAGE

Easy-To-Use Tools And A Symbiotic Relationship With Neural Networks Will Make The Difference.

BY JACK SHANDLE

In the engineering workplace, where a high value is placed on precise reasoning, mathematical formulations, and "crispness," a technology as holistic in concept as fuzzy logic was certain to encounter rough sledding. Even successes in several consumer applications, such as appliances and hand-held video cameras, made only a small dent in the prejudice against fuzzy logic.

For the companies that know how to use it, the simple fact is that fuzzy logic has been deemed a technology that provides a strategic advantage in the marketplace. Understandably, these companies haven't been falling over themselves to publish hard data substantiating their success stories. Most likely, though, they feel quietly satisfied when microcontroller-industry pundits make a case against it *(see "What's all this fuzzy logic stuff, anyhow?",* ELECTRONIC DESIGN, *May 13, p. 77, Nov. 1, p. 95, and Nov. 11, p. 105, 1993).*

As in most areas of human endeavor, fuzzy logic isn't a black-and-white issue. A case can be made against adopting it in a sweeping, broad-brush fashion. Fuzzy logic historically has had more than a few critical problems. As systems become more complicated and more complex, it becomes difficult to determine the right set of rules and membership functions *(see "Facts on fuzzy logic," p. 80).*

A good deal of time has been spent in front-end design to properly tune the membership functions and adjust the rules, as needed. Human beings, for example, experience cognitive overload when the system requires more than six or seven rules to describe it properly. For extremely complex systems, it has been a daunting challenge to find any kind of solution. But it should be remembered that conventional systems using crisp logic have a similarly tough time.

The very fact that the flow of fuzzy-logic products is consistently growing can't be ignored, however. To some degree, the application of this technology has been retarded not just by its problems, but by a lack of intuitive, development tools and by the learning curve for any new technology.

In the right application, the advantages of fuzzy logic include quicker development cycles and superior performance. Typically, conventional control solutions have five development steps: developing a model of the system, developing a mathematical model for the controller, analyzing the equations, converting the model to a circuit, and building the circuit. Fuzzy logic, on the other hand, has just three: developing the fuzzy model, then simulating and compiling it *(Fig. 1).*

It's in the realm of solving design problems, where nonlinear, time-varying functions can't be acceptably approximated by crisp logic, that fuzzy logic has an advantage. Because it provides answers without having to create an equation that precisely models the system's behavior, this also means a shorter development cycle.

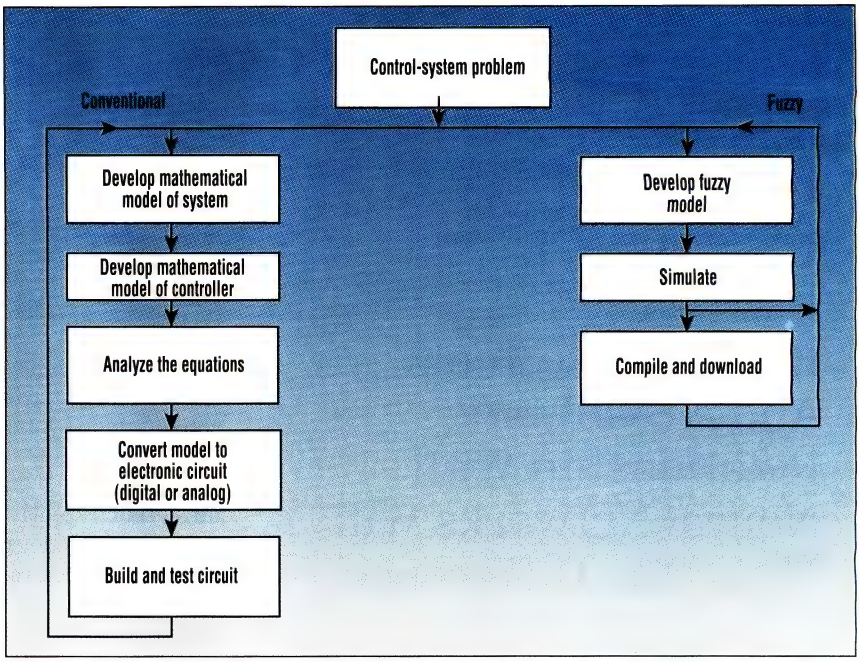
But the primary problem has been that as more rules govern the system, the time needed to identify and create the rules rises exponentially. As a result, there's been a relatively narrow range of applications that fuzzy logic can address, and these tend to be in the consumer-products arena.

Generating rules and membership functions for fuzzy logic is essentially a learning process, however. A number of articles published recently in academic journals, and papers delivered at conferences, thus propose using another artificial-intelligence technology—neural networks. Such networks assume that front-end learning process.

Neural networks and fuzzy logic have complementary strengths. Using supervised learning, a neural network can "sort out" the rules and membership functions that make a system behave as the designers wish. Fuzzy logic, on the other hand, is an ideal technology for low-cost implementation.

In Yokohama, Japan, researchers at the International Fuzzy Engineering Research Laboratory designed an inference message that allows fuzzy-logic parameters to be tuned by a back-propagation neural network. The system teams the effect of many rules into aggregate operators that are tuned by the neural network. One system for foreign-exchange trade support is said to consist of 5000 rules.

In the U. S., Ford Motor Co., Dearborn, Mich., combined fuzzy logic and neural networks in its research on an idle-speed control system for cars. Instead of the usual membership functions and inference structure, Ford Motor Co.'s researchers used differential approximations of those two parameters, which allowed the neural network to learn. When compared to a traditional proportional-integrated-differential (PID) controller, the neural/fuzzy solution performed better, especially under varying load conditions.


Control-system problem
Conventional
Fuzzy
Develop mathematical model of system
Develop mathematical model of controller
Analyze the equations
Convert model to electronic circuit (digital or analog)
Build and test circuit
Develop fuzzy model
Simulate
Compile and download

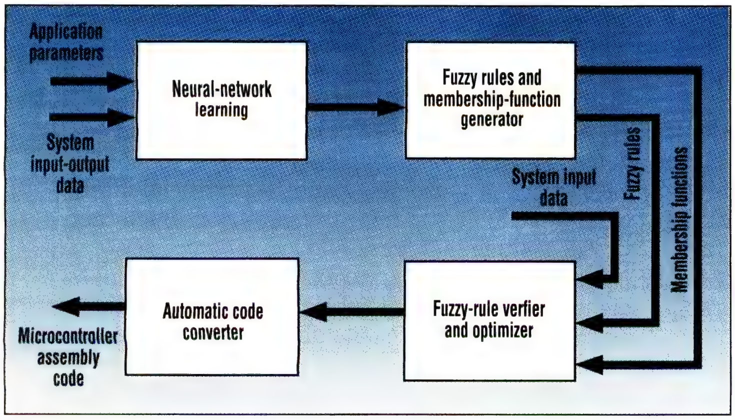
1. Conceptually, the solution of a typical control-system problem can be accomplished in fewer steps using fuzzy logic instead of conventional techniques. But the range of applications for fuzzy logic has historically been limited to a narrow range of highly nonlinear, time-varying functions that don't require *too* many fuzzy-logic rules.

One of the first neural-fuzzy technologies to step beyond the academic realm is National Semiconductor Corp.'s NeuFuz, the brainchild of Emdad Khan, head of Intelligent Systems in the Embedded Systems Division. NeuFuz's major advantage is that it can create membership functions higher in complexity than the linear relationships fuzzy-logic designers have used up until now. NeuFuz accomplishes this by having the neural network generate exponents for the equations that describe the nonlinear membership functions *(Fig. 2)*.

Architecturally, the front-end neural network can be implemented in as few as three layers, each addressing a key segment of the fuzzy-logic methodology. The first layer of neurons performs fuzzification, the second creates the rule base, and the third layer—a single neuron—does rule evaluation and defuzzification.

Training the neural network consists of supplying inputs and demanding the specific output. The neural network achieves this primarily by adjusting the weights in the connections between neurons in different levels until the complete set of inputs and their correct outputs is obtained. Because the number of neurons in the first layer of the neural network can be almost arbitrarily set, the amount of input variables isn't limited and the number of rules, which are created in the second layer of the neural network, can also be extensive.

It's obvious that a neural network is set up to create (or emulate) a fuzzy-logic controller, and could be used in the recall mode to implement the end-user application. But speaking in practical terms, it's not a good idea to leave the implementation in this form. Neural networks are simply too computationally intensive and require significant hardware investments to work in the response times required by the applications. So the National Semiconductor solution includes the capability to generate assembly code for a strictly fuzzy-logic solution. Once in this form, the solution can run on an inexpensive microcontroller instead of some parallel-processor architecture.



2. A neural network employed as a front-end learning system for a fuzzy-logic controller can tackle the difficult tasks of forming fuzzy-logic rules and membership functions for complex problems. Adding a means to convert the neural-network solution to a 100% fuzzy-logic solution that runs on a low-end controller completes National Semiconductor's NeuFuz technology.

NeuFuz provides the migration path needed by fuzzy logic to go beyond a relatively narrow range of applications. These applications, on the one hand, typically are too complex for conventional Boolean-ori-

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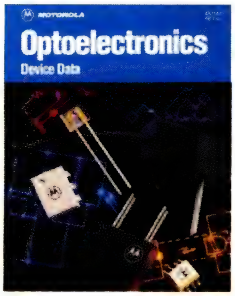

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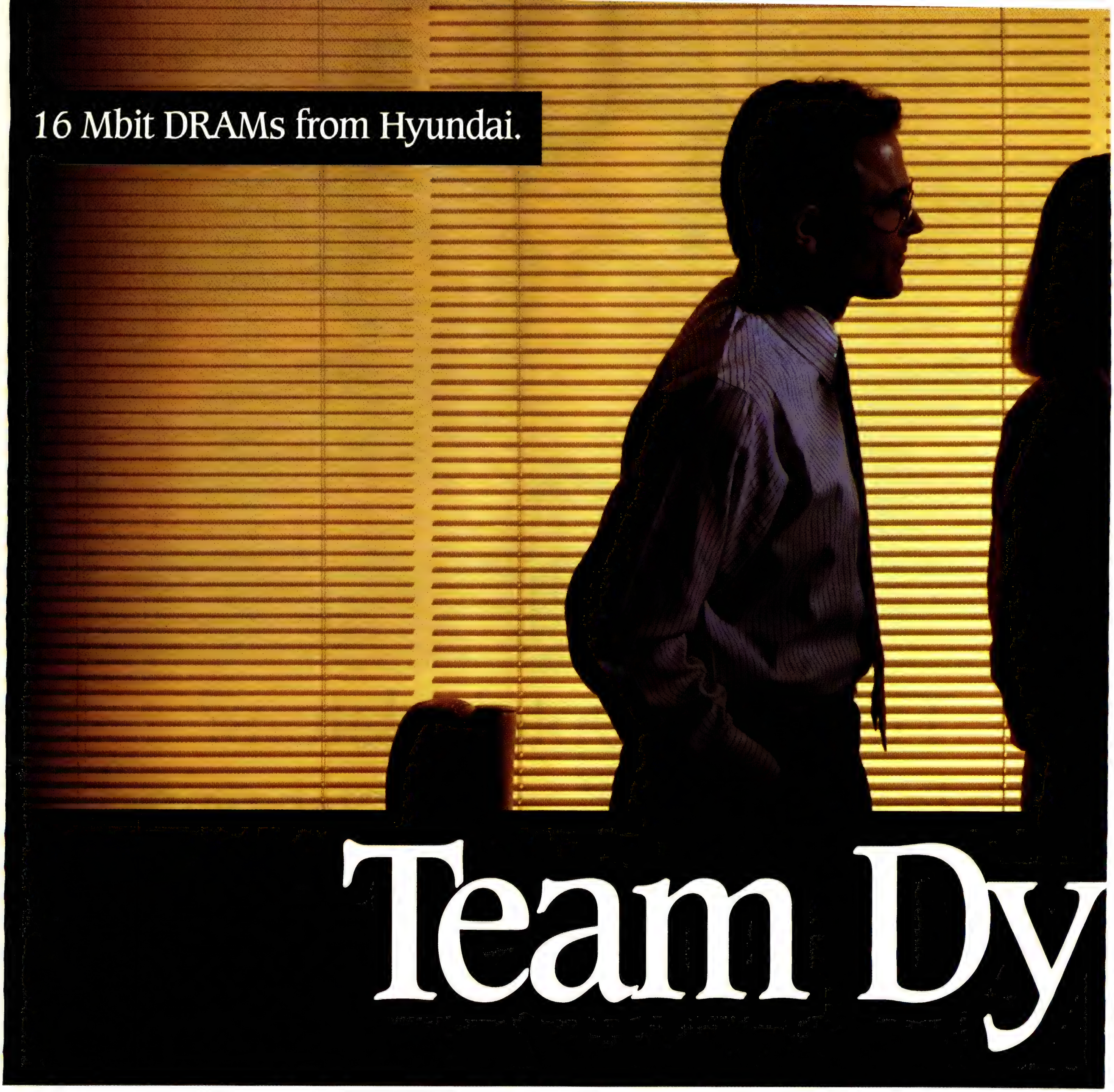
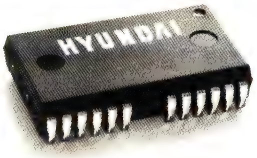


16 Mbit DRAMs from Hyundai.

Team Dy



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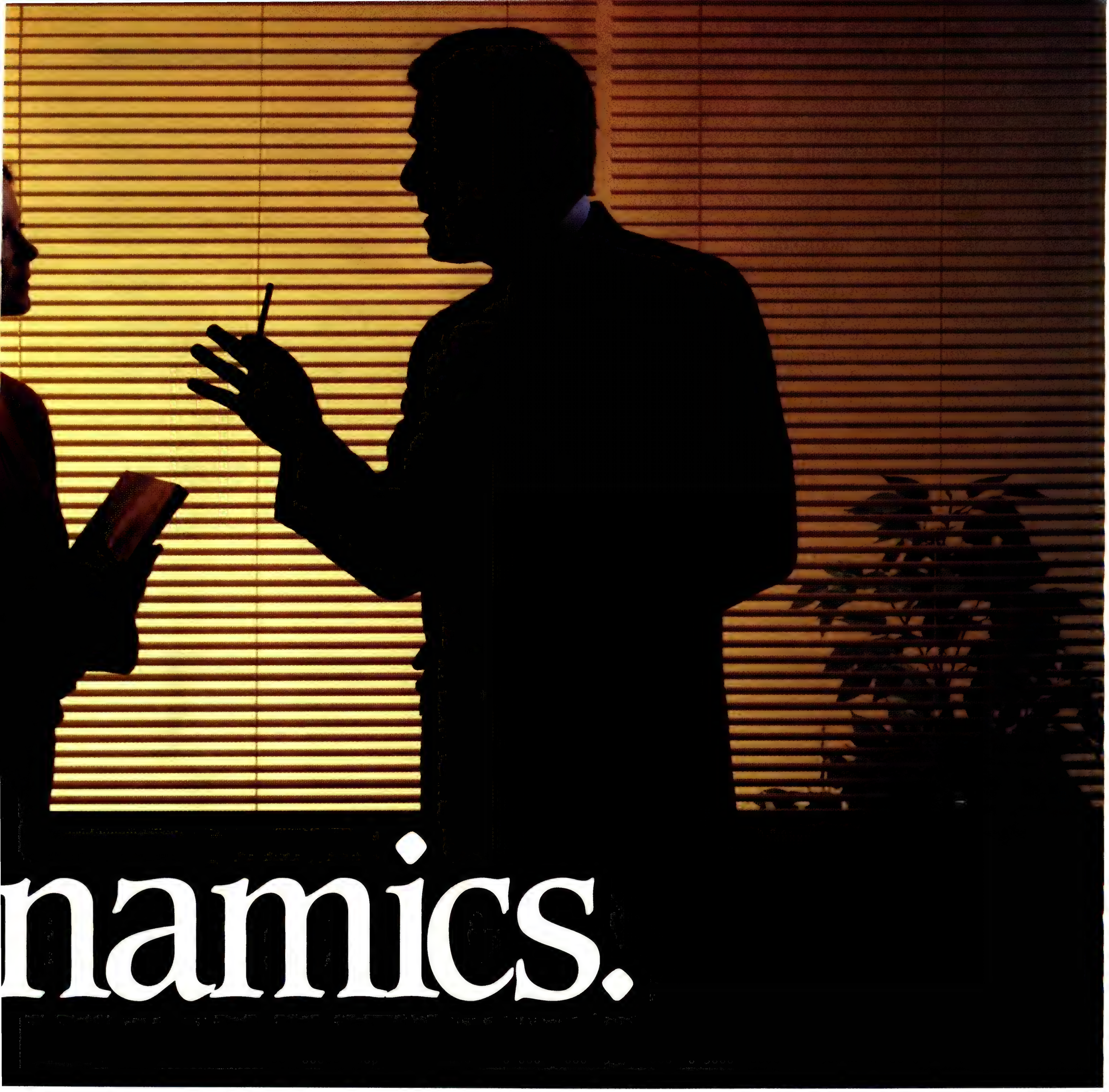
Your Hyundai DRAM Source Guide

Size	Part Number	Speed ns	Refresh Cycles/ms	Production
16M x 1	HY5116100	60/70/80	4096/64	now
	HY5117100		2048/32	
4M x 4	HY5116400	60/70/80	4096/64	now
	HY5116410		4096/64 WPB	
	HY5117400		2048/32	
	HY5117410		2048/32 WPB	
2M x 8	HY5116800	70/80	4096/64	Q4 '94
	HY5116810		4096/64 WPB	
	HY5117800		2048/32	
	HY5117810		2048/32 WPB	
1M x 16	HY5116170	70/80	4096/64	Q4 '94
	HY5116370		4096/64 WPB	
	HY5117370		2048/32 WPB	
	HY5118370		1024/16 WPB	
	HY5116260		4096/68	
	HY5117260		2048/32	
	HY5118260		1024/16	
	HY5116460		4096/64 WPB	
	HY5117460		2048/32	
	HY5118460		1024/16 WPB	

All available in standard and low power versions.
Packages include SOJ, TSOP II, reverse TSOP II.



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Hyundai's new DRAMs feature speeds of 60, 70, or 80 ns. Immediately available, the HY5116100 and HY5117100 are organized 16M x 1 and provide 4096 refresh cycles per 64 ms and 2048 refresh cycles per 32 ms, respectively. New 4M x 4 parts include the HY5116400, with 4096 refresh cycles per 64 ms, the HY5116410 with write-per-bit capability, and the HY5117400 and write-per-bit capable HY5117410 offering 2048 refresh cycles per 32 ms.

All parts are available in standard and low power versions, dissipating 495 mW operating at 60 ns, 440 mW at 70 ns, and 385 mW at 80 ns. Other features include operation from a single 5V ±10% power supply, TTL compatible inputs and outputs, fast page mode operating, multi-bit test capability, read-modify-write capability, and CAS-before-RAS, RAS-only, as well as hidden refresh. Packages include standard 24/28 pin plastic, TSOP II, and reverse TSOP II. TSOP will be available soon.

These new parts are products of Hyundai's 0.55 micron CMOS process, at one of the most advanced electronics manufacturing plants in the world. So if purchase of 16 Mbit DRAMs is on your agenda, and you don't want to get caught short the way some did on 4 Mbit, start the team dynamics now.

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ented microcontroller solutions. On the other hand, they're too difficult for conventional fuzzy-logic techniques. National Semiconductor's Khan has, for example, mapped strategy for solving problems as difficult as continuous-speech recognition using NeuFuz technology.

After many years of trying, researchers in continuous-speech recognition have settled on the Hidden Markov Model (HMM) method as being the best to-date. HMM uses statistical pattern recognition as its core technology, recently teaming it with neural-network technology to handle the compute-intensive task of modeling statistical distributions of audio frequencies that characterize speech. Although Khan hasn't disclosed his plans in detail, it seems likely that they will be based on using a neural network capable of modeling a fuzzy-logic system as the front end to the HMM.

Whereas NeuFuz promises to take fuzzy logic to the next plateau in terms of problems it can solve successfully, products from other companies continue to make significant progress in making "mainstream" fuzzy logic less intimidating. In the past year or so, most companies marking fuzzy-logic products have tuned their strategic position by offering development tools complete with sophisticated graphical user interfaces and visualization capability. American NeuraLogic Inc., San Jose, Calif., for example, created a Windows-based development systems called INSiGHT that produces code for the company's NLX22x family of fuzzy-logic processors.

INSiGHT's model editor creates and edits models of fuzzy-logic microcontrollers. The input editor generates the data files needed for simulations, and the simulator runs the simulations. An output viewer analyzes the simulation output files so users can fine-tune their fuzzy-logic models. The models run on the company's dedicated chips. A unique feature of NeuraLogic's NLX220 is a floating membership function. As the name implies, this function lets users change the center and width values of their membership functions.

Similarly, one of the market leaders, Togai InfraLogic Inc., Irvine, Calif., late last year introduced its TTLShell 3.0, a Windows-based software devel-

FACTS ON FUZZY LOGIC

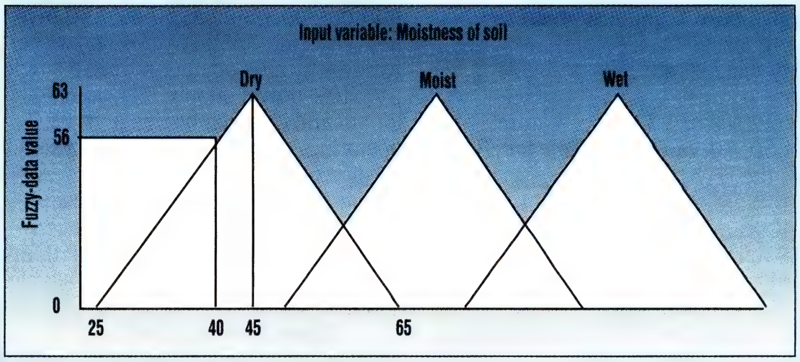
Fuzzy logic is not crisp. It does not view the world through Boolean eyes. Rather, fuzzy-logic methodology, a branch off of artificial intelligence, is basically characterized by three traits:

- It does not consider whether something is true or false, but rather how true the statement (about a parameter) is.
- Because it's similar to human reasoning, its implementation tends to be based on natural language.
- It's flexible and can model complex, nonlinear systems by using imprecise information.

Conceptually, fuzzy logic requires a paradigm shift from Boolean-based solution methodologies. What's presented here is more of a primer on the fundamentals of the technology. One of the basic ideas behind fuzzy logic is the concept that a set of imprecise rules can be written to describe how the system being modeled behaves. The interaction between the rules eventually produces an answer that carries with it a degree of confidence in its correctness. The rules are written in natural language, and they relate inputs to outputs.

Another basic concept is that of membership functions, which compare and classify input data. Membership functions act on input variables, usually from sensor data, in what's known as a fuzzifier. The fuzzifier's output is referred to as a fuzzy-data value, and as a general rule, the membership functions are chosen to be simple "shapes," such as triangles and trapezoids. For example, the designer might want to represent the degree of moistness in soil with a membership function, using three "triangles" consisting of up-and-down ramp functions *(see the figure)*.

The fuzzy-data value becomes the input of the rule evaluator, which compares the fuzzy-data value to values established for each rule. Rules are formulated in terms of the inputs, and all describe factors governing how the system acts. If one rule seems to be the dominant explanation for the fuzzy-data value, it's considered to have "won." This news is passed on to a defuzzifier, which is also known as a response calculator. The defuzzifier sends a direction formulated in Boolean mathematics to the microcontroller. The mode that has just been described provides an immediate output. But the decision can also be placed in another mode in which successive input values are accumulated and analyzed before a direction is given.



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opment tool. Based on Computer-Aided Software Engineering (CASE) concepts, TTLShell 3.0 offers real-time debugging and tuning of fuzzy rules, membership functions, and rule weights. A 3D color visualizer provides better insight into rule-base tuning. In addition, the tool provides advanced fuzzy-inference methods that include S-shaped membership functions—another departure from the linear functions typically used by designers.

In the past, fuzzy-logic solutions have run almost exclusively on microcontrollers. The choice essentially falls between standard, off-the-shelf parts and faster, dedicated fuzzy-logic microcontrollers, such as those offered by NeuraLogic and Togai. Now another hardware option is being proposed by Texas Instruments, with its introduction of software development tools that target the company's TMS320 digital-signal-processor chips.

TI's DSP marketing manager, Kun-Shan Lin, claims that implementing fuzzy solutions on DSP ICs can provide a ten-fold performance boost over a comparably-priced, off-the-shelf, 16-bit microcontroller. The DSP solution is roughly equivalent in performance to the dedicated fuzzy-logic controllers. Since input data for high-end fuzzy systems (e.g., signal analysis) often must be collected and processed before being handed off to the microcontroller, the DSP approach offers the benefit of doing both functions on one chip. Traditionally employed for handling signal-processing problems, a DSP IC simply uses spare computational bandwidth for the fuzzy-logic control functions.

A new hardware option requires new software development tools, of course, so TI teamed up with Inform Software Corp., Evanston, Ill., to deliver the TMS320fuzzyTECH logic tools. Just as with competing products, these tools offer a full graphical environment. They generate code for TI's TMS320C2x and TMS320C5x family of DSP ICs. The generalized fuzzy system created by the software is linked to existing applications and called like a standard C function. But its performance actually is comparable to highly optimized assembly code. In TI's solution, a fuzzy system with 20 rules, 2 input variables, and 1 output typically needs about 870 bytes of ROM and 27 bytes of RAM. Running on a TMS320C50 DSP IC, the system would need 0.024 ms to compute.☐

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Commonly Used Packages	16SOIC	20SOIC	44PLCC	68PLCC	84PLCC	100PQFP	128PQFP	144PQFP	160PQFP	160PQFP	208PQFP
	14SOIC	16SOIC	28PLCC	44PLCC	68PLCC	84PLCC	100PQFP	100PQFP	144PQFP	144PQFP	160PQFP
		14SOIC	20SOIC	28PLCC	44PLCC	68PLCC	84PLCC	84PLCC	100PQFP	100PQFP	144PQFP
			16SOIC	20SOIC	28PLCC	44PLCC	68PLCC	68PLCC	84PLCC	84PLCC	100PQFP
							44PLCC	44PLCC	68PLCC	68PLCC	84PLCC
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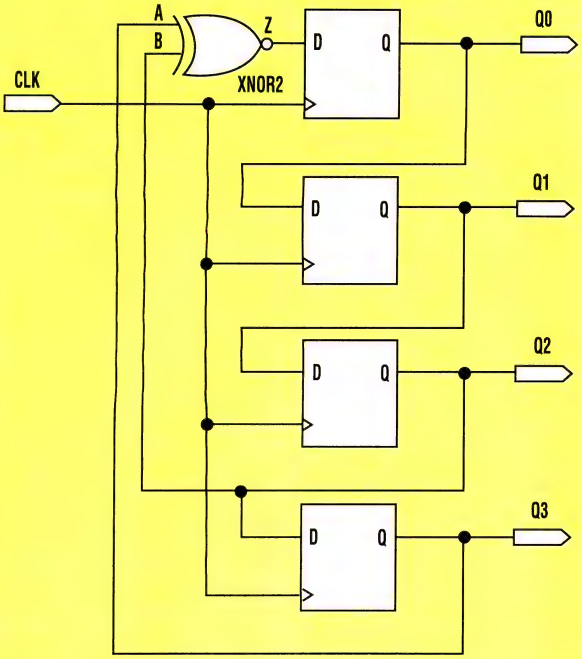


PSEUDORANDOM COUNT SEQUENCE

State #	Q3	Q2	Q1	Q0	Q3/Q2 XNOR	HEX
State 0	0	0	0	0	1	$0
State 1	0	0	0	1	1	$1
State 2	0	0	1	1	1	$3
State 3	0	1	1	1	0	$7
State 4	1	1	1	0	1	$E
State 5	1	1	0	1	1	$D
State 6	1	0	1	1	0	$B
State 7	0	1	1	0	0	$6
State 8	1	1	0	0	1	$C
State 9	1	0	0	1	0	$9
State 10	0	0	1	0	1	$2
State 11	0	1	0	1	0	$5
State 12	1	0	1	0	0	$A
State 13	0	1	0	0	0	$4
State 14	1	0	0	0	0	$8
Then sequence repeats . . .						

1. THE COUNT SEQUENCE of a 4-bit linear feedback shift register (LFSR) has a maximum of 2^N–1 states. One state, referred to as the lockup state, is lost.

LINEAR-FEEDBACK SHIFT REGISTERS RAMP UP COUNTER PERFORMANCE WITHOUT SACRIFICING TOO MUCH ROUTING AND LOGIC DENSITY.

USE LFSRS TO BUILD FAST FPGA-BASED COUNTERS

Complex PLDs (CPLDs) currently represent the workhorses for 10- to 16-bit counter designs running at 80 to 100 MHz. These CPLD-based designs are largely based on a conventional binary-counter approach, because the devices' sum-of-products architecture and wide product-term inputs are ideal for implementing traditional binary counters.

The design of larger, faster synchronous counters based on either CPLDs or field-programmable gate arrays (FPGAs), however, is fraught with speed and density trade-offs. For example, when CPLD expander product terms or other architectural features are employed for larger counters, engineers incur additional propagation delays and sacrifice performance. Also, CPLDs typically have far fewer available registers than FPGAs. As a result, any large counter consumes a much greater

BOB KLEIN
AT&T Bell Laboratories, 10500 Little Patuxent Pkwy., Suite 400, Columbia, MD 21044; (410) 992-0937.

percentage of the available on-chip logic resources. With second-generation SRAM-based FPGAs, the limited routing resources and the narrow input-logic blocks confine their ability to efficiently implement large, fast binary counters.

Some CPLD and FPGA vendors try to resolve these issues by including hardware and architectural enhancements, such as fast carry logic and/or wide decode logic. But these solutions add to the total propagation delay. Each bit that's carried or cascaded tacks on a nanosecond or two, which degrades performance as counter length increases. Consequently, engineers that venture into FPGA terrain in hopes of optimal counter designs experience the same speed/density limitations they do with CPLDs.

Ideally then, the engineer's best avenue is dedicated circuitry for counters that doesn't consume routing resources external to the basic logic element. The size of the logic element needs to balance the conflicting goals of flexibility (best implemented with small or fine-grain logic blocks) and functionality (best implemented with large or course-grain logic blocks). That's what third-generation SRAM-based FPGAs provide through a multigrain, configurable lookup-table (LUT) architecture *(see "Fixed vs. multigrain LUTs," below).*

This architectural feature coupled with a counter-design technique called maximal-length linear feedback shift registers (LFSRs) overcomes fast counter design limitations. In fact, such an FPGA-based design can yield counter speeds of 100 MHz and beyond without consuming inordinate logic and routing resources.

LFSR OPERATION

An LFSR operates on the same principle as a Johnson counter. Correctly selected bits, referred to as taps, are fed back through an exclusive NOR (XNOR) or exclusive OR (XOR) to form the least-significant-bit (LSB) input.

An LFSR sequences through a maximum of $2^N–1$ states, losing one state that's referred to as the lockup state. A traditional binary counter, on the other hand, cycles through 2^N states where N is the number of bits or registers in the counter. For example, an 8-bit binary counter has 256 states (255 plus zero); a maximal-length LFSR can produce a non-repeating sequence of 255 states. The output states of the LFSR, however, aren't sequential but rather pseudo-random *(Fig. 1).*

The beauty of the LFSR implementation in an FPGA is that only a few bits need to be fed back to achieve a maximal-length sequence. This lends itself perfectly to a configurable FPGA architecture due to the limited routing resources available. By way of comparison, an N-bit binary counter, even if implemented with T (toggle) type registers, would still require N terms at the Nth bit to define the toggle state. With each of these terms requiring a routing resource, it's easy to see why routing can become a limiting factor when implementing large counters in field

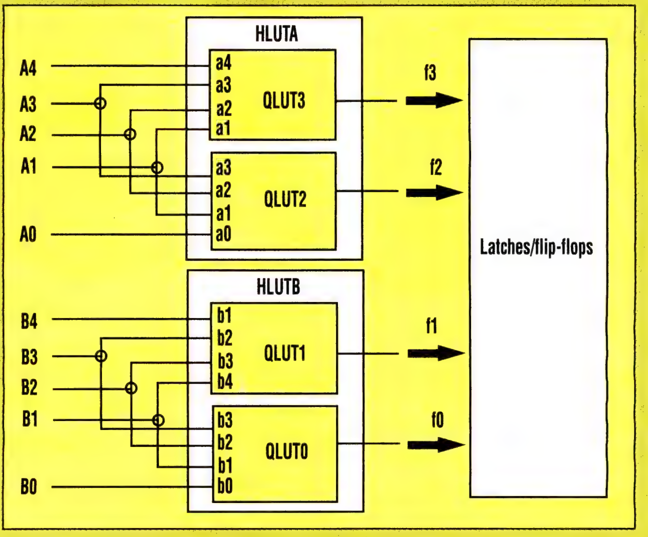
FIXED VS. MULTIGRAIN LUTs

Conventional FPGA look-up-table (LUT) architectures are limited to 4-input functions, which are regarded as the most efficient for area density. However, multigrain LUTs (like those in AT&T's ORCA devices) can be used in different modes to meet various logic requirements *(see the figure).* The LUT's configurable medium- to large-grain architecture can implement from one to four combinatorial- or registered-logic functions. In addition, the multigrain LUT handles wide-input functions and multiple, smaller-input functions to maximize the gate count for each programmable function unit (PFU).

Multigrain LUTs can be arranged to perform random logic functions with 4 to 11 inputs, or nibble-wide functions like adders and counters. Moreover, changing the LUT's grain to create 4-, 5-, and 6-input independent look-up tables gives engineers great latitude to implement a wide range of functions.

Engineers also can opt to use the 64-bit LUT in each programmable logic cell (PLC) as one 16-by-4-bit SRAM element, two 16-by-2-bit SRAM elements, or one 16-by-2-bit SRAM element combined with a 5-bit function or two 4-bit functions.

Lastly, but of particular importance for fast-counter designs, the nibble-wide ripple mode provides engineers with the ability to implement 4-bit arithmetic functions. The fast-carry circuit in each programmable function unit gives engineers the extra speed edge to cascade these four-bit functions in the linear-feedback-shift-register application or any similar design. In addition, dedicated fast-carry routing resources exist between programmable logic cells so that 8-, 16-, 32- or 64-bit arithmetic, shifter, and counter functions are possible.



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programmable gate arrays.

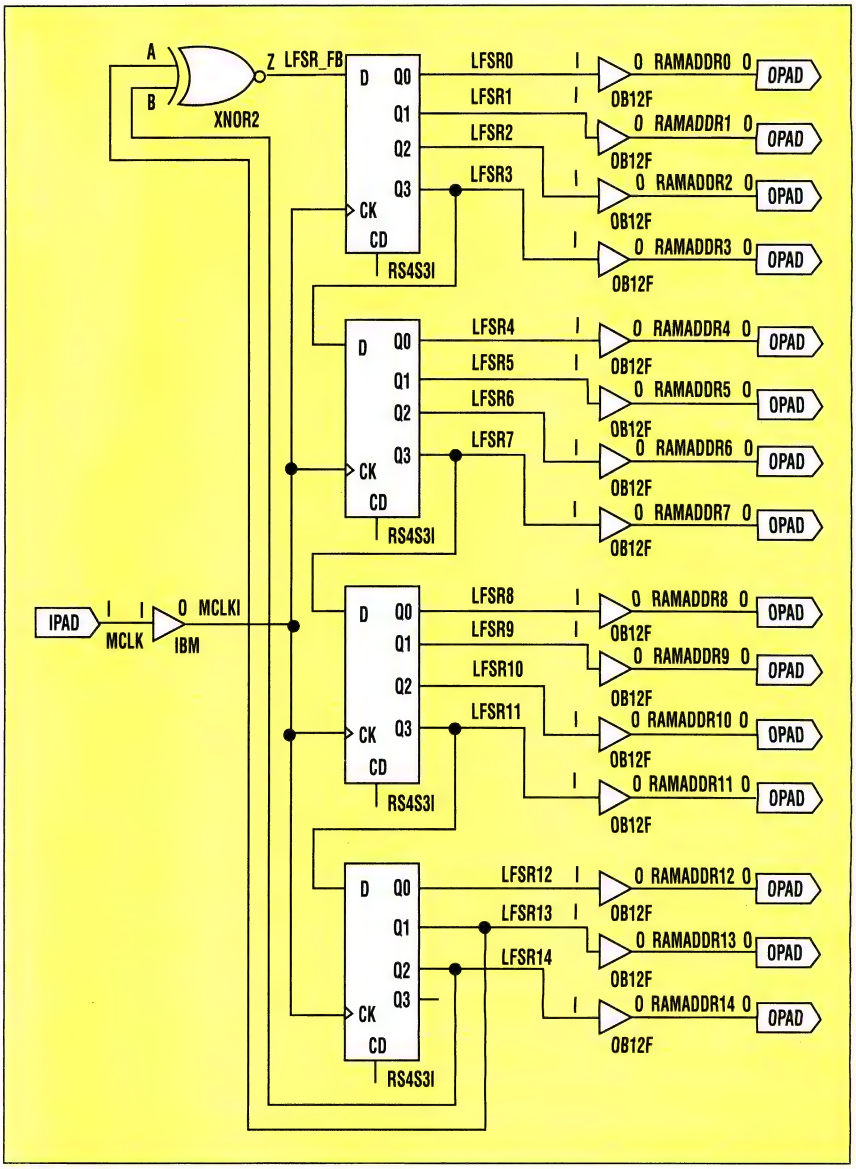
Engineers give up one state (255 vs. 256 for N=8, for example) when using LFSRs, because that state will make the LFSR lock up. To illustrate, assume the counter in Figure 1 is loaded with all logical 1s. The XNOR of bits Q3 and Q2 is also a 1. Therefore, if this counter were to enter this state, it would continue to simply shift all 1s until forced out of this lockup state through reset or some other mechanism.

This example shows why XNOR feedback rather than XOR feedback is generally preferred in FPGA-based LFSR implementations. Because most FPGA registers power up to a 0 state, selecting XNOR feedback ensures the LFSR won't power up in the lockup state. Some third-generation SRAM-based FPGAs, like AT&T's Optimized Reconfigurable Cell Array (ORCA) devices, can have each register individually configured to power up and/or reset to a known state (either a 1 or 0). This eliminates the possibility of powering up in the lockup state and allows either XOR or XNOR feedback to be utilized effectively.

AN LFSR DESIGN

As a first step in this design flow, engineers should determine whether or not an LFSR will actually work in a given application. If a counter design absolutely needs a binary or decimal count sequence, this technique won't work. But in a number of applications, such as circular buffer address generators, FIFO read/write pointers, and frequency dividers, LFSRs are highly efficient.

LFSR counters are ideal for functions with sensitive analog circuitry, like an address generator for an analog-to-digital-converter circular buffer memory (as in a storage oscilloscope). This is because LFSR counters generate far less noise than their binary cousins. Because the output sequence is pseudorandom, simultaneous-switching noise is nonperiodic over the spectrum of dc to 1/Nt, where N is the number of bits and t is the clock period. Conversely, the noise generated by binary counters is coherent and periodic, with large amounts of energy generated when a number of logical 1s roll over to 0s, such as a 16-bit counter rolling over from $FFFF (hex) to $0000 (hex). In this same counter example, lesser but still significant noise pulses are generated when other transitions occur, such as $7FFF to $8000 and $3FFF to $4000.



2. THIS SCHEMATIC SHOWS a 15-bit, maximal-length, LFSR-based counter. An LFSR works like a pseudorandom number generator: one stage shifts to the next and certain bits are fed back through an XNOR to form the least-significant-bit input.

While it may initially appear that an LFSR won't work in some counter designs because of the pseudorandom output, it can still be used by decoding the output to the corresponding binary count. Typically, that can be performed off-line, either through an attached microprocessor or an LUT. Because the LUTs in the ORCA FPGAs are also usable as RAM or ROM blocks, this decoding can actually take place on-chip.

A schematic entered with ViewDraw from Viewlogic Systems shows an FPGA-based, 15-bit, maximal-length LFSR counter that can operate at over at 100 MHz *(Fig. 2)*. The resulting FPGA application netlist (FAN) file is processed with map, placement, and routing (MPR) tools in AT&T's ORCA Development System (ODS) to obtain the completed implementation, including a bit stream for programming the selected FPGA device. The Timing Analyzer in ODS verifies the performance of the routed design, and reports the

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```
*** DESIGN INFORMATION ***
________________________________________________________________
File Name:                    lfsr2.rpt
Device Type:                  ATT1C05-2
Timing Condition:             Commercial: Vcc = 4.75V, Temp = 70 C

Notes:
1. All delays are for the worst-case temperature and voltage.
2. All output delays are based on 50 pF loading.
3. All latches are modeled as edge-triggered devices with the latching edge acting as the trigger.
4. The global set/reset (GSR) paths are NOT included in the timing analysis. Please refer to the data
   sheet for delay information regarding the global set/reset.

*** TIMING ANALYSIS ***
________________________________________________________________
Maximum Operating Frequency:
MCLKI                                  137.1 MHz
```

maximum operating frequency at 137.1 MHz *(see the listing).*

The ORCA device is the FPGA architecture used in this article's LFSR example. It's SRAM-based, and is architecturally homogeneous and symmetrical, meaning that each logic block or programmable logic cell (PLC) is exactly the same across the array *(Fig. 3).* Symmetrical refers to maintaining the same number and type of logic and routing elements in the horizontal and vertical directions. With this symmetry, a shift register or counter chain implemented in a horizontal orientation may be switched to a vertical implementation with no change in the number or type of routing resources used, and with no effect on the timing of the function.

The LFSR-based counter design is implemented in an ATT1C05, a device with 5000 usable gates and 576 registers organized into 144 PLCs. Each PLC contains a programmable function unit (PFU) and routing resources. The PFU itself consists of a 64-bit LUT, intermediate logic to combine the sections of the LUT (for functions of up to 11 inputs), and four configurable latches/registers. The LUT can be configured as one 64-bit LUT, two 32-bit half LUTs, or four 16-bit quarter LUTs (QLUTs) *(Fig. 4).* Each QLUT has dedicated carry logic to route a fast carry signal to and from adjacent QLUTs *(Fig. 5).*

By using internal carry circuits, engineers can implement a fast, 4-bit counter function in one PFU. Also, each PFU has carry-in (CIN) and carry-out (COUT) ports for fast carry routing between adjacent PFUs. Because of the device's symmetry, the PFU-to-PFU carry chains can propagate top-to-bottom, bottom-to-top, left-to-right, or right-to-left with equal speed and efficiency.

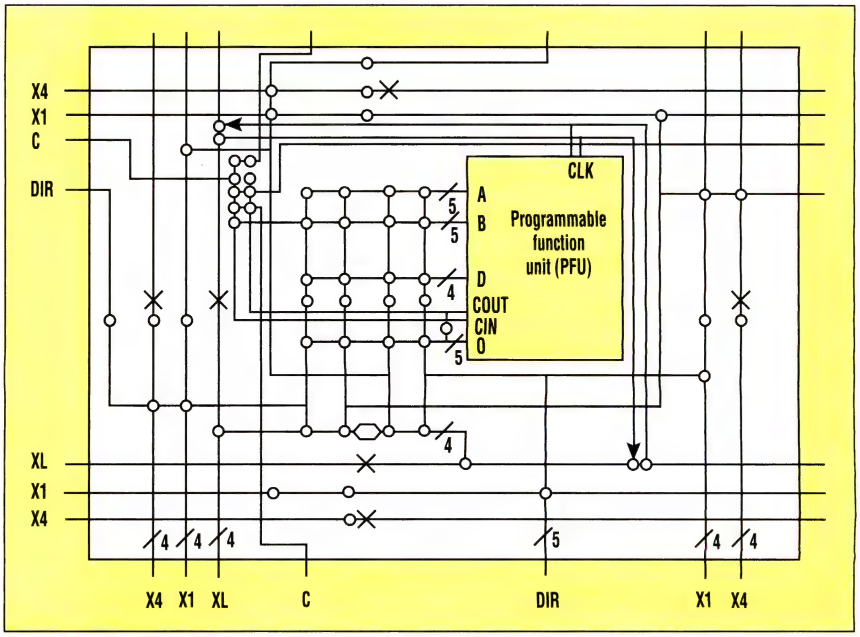
The LFSR is a straight shift register (SR) with the most-significant bit (MSB) and at least one other bit fed back through a XNOR gate to form the input to the SR's LSB. This design takes advantage of the FPGA's fast carry chain to implement the shift registers.

Feedback bits for a 15-bit counter are bits 15 and 14. Because these are adjacent bits, they can use identical, fast, local routing resources to reach the XNOR function that's implemented in the QLUT in front of the LSB register.

Four PFUs are used to implement the 15-bit counter and the XNOR gate, which generates the input signal to the counter's LSB. The PFUs used for the SR functions are placed sequentially to deploy the fast-carry resources for sequential bit connection in the SR chain. Because only a few bits need to be fed back, the number and complexity of routing resources required are significantly lower than for a binary counter, even when using T-type registers.

LIBRARY ELEMENTS

The design then involves choosing the library elements that utilize the fast carry circuits in the ATT1C05. Four RS4S3I 4-bit shift-register macros from the ORCA library are cascaded to obtain the needed length. For maximum speed at the I/O ports, the OB12F output buffer elements are selected. These buffers offer the fastest of the three output switching times available with the devices, and provide 12 mA of output sink current. Only three PFU-to-PFU fast carry routing resources are required; all other carries are bit-



3. THE FPGA ARCHITECTURE best suited to LFSR counter design is homogeneous and symmetrical. In other words, each programmable logic cell (PLC) is exactly the same across the cell array. Also, the same number of logic and routing elements are in the horizontal and vertical directions. This PLC contains a programmable function unit (PFU) and routing resources.

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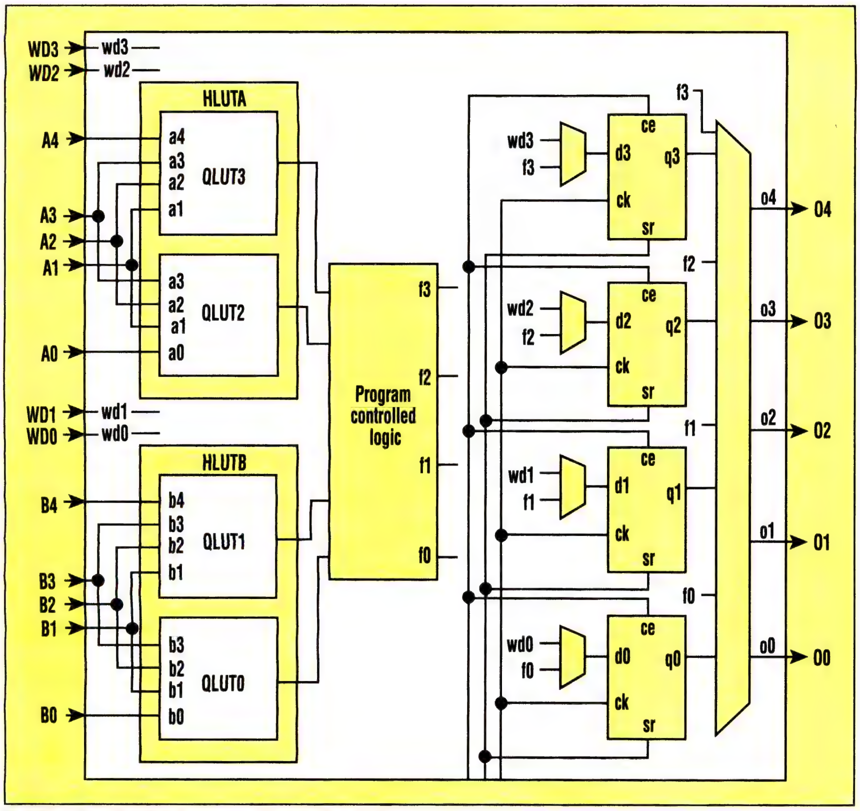


4. EACH PROGRAMMABLE function unit contains four registers and a 64-bit lookup table (LUT). The LUT can be used as is, or configured into half and quarter LUTs.

to-bit using the dedicated carry logic within the PFUs.

The outstanding performance of LFSR counters compared to traditional binary counters lies in the fact that the fast carry resources only need to propagate from one bit to the next. In a binary counter, for the carry signal to reach the MSB, it must propagate through all lower-order bits. Even with dedicated fast-carry resources, the cumulative propagation delays of the lower-order stages will be the limiting factor in binary-counter performance.

LIMITING FACTOR

In the LFSR, the limiting factor is the routing delay from the feedback taps combined with the LUT delay to form the XNOR function of these taps. While this design operates at over 120 MHz, a 15-bit conventional binary counter in the same device has a top speed of around 60 MHz. The new 0.5-µm ATT2CXX device family extends binary-count speed to over 80 MHz and density to over 22,000 usable gates.

The shift-register design may be entered with a schematic or with text entry. With text entry, the entire design can be described in just a few lines of code:

```
Q[14:1]:= Q[13:0];
  Q[0]:= Q[14] XNOR Q[13];
```

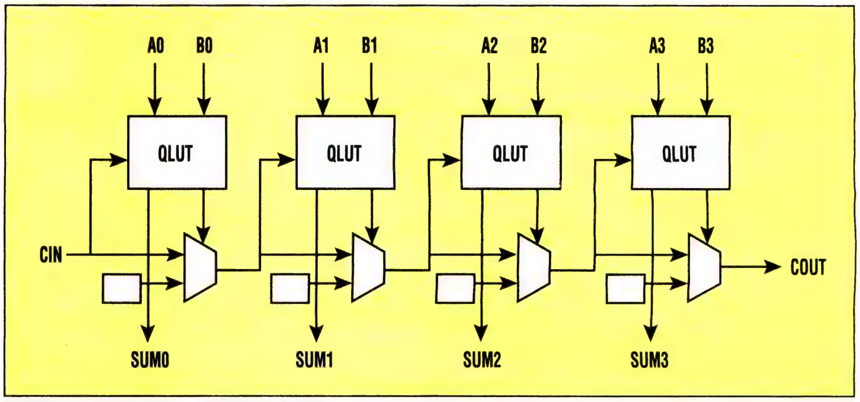
The syntax here is generic, but could easily be modified for any popular synthesis language. Line one essentially performs the shift-left (LSB toward MSB) function. Line two creates the LSB from the XNOR of the two most significant bits.

Engineers must determine which bits to feed back through the XOR/XNOR to achieve a maximal length sequence *(see the table)*. Feedback connections in the table aren't necessarily unique; other tap selections may also result in maximal length sequences. Many digital-electronics text and reference books and application manuals offer similar charts. In addition, a computer program available on the AT&T Bulletin Board (215-778-4314) will calculate which taps will produce maximal length sequences for counter lengths up to N=32. The same program can take a given length LFSR and calculate the output bit pattern for any particular count. This is especially useful when designing programmable frequency dividers based on modulo-N division.

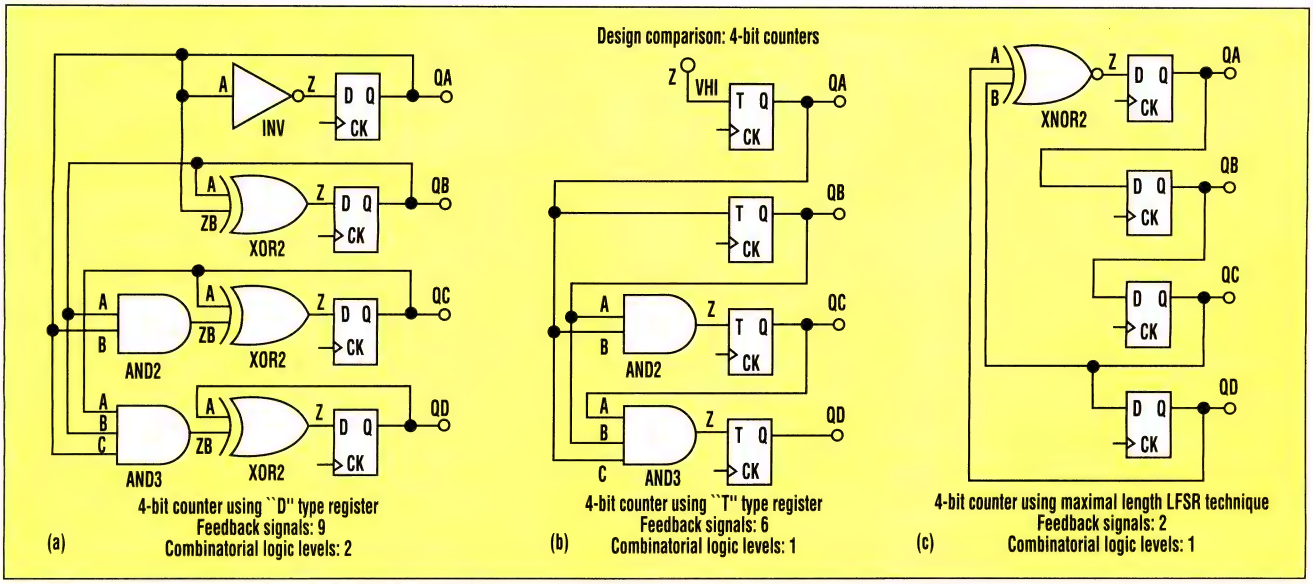
WHY FPGAS?

Designing binary counters with complex PLDs is a simple process using either schematics or text. By combining CPLD sum-of-products architectures with the high level of connectivity, counters with a relatively high number of bits can be implemented in a traditional method *(Fig. 6a)*. The number of signals that must be fed back to implement a given length counter increases as a function of the number of bits.

For example, at the fourth bit, all three previous bits plus the current



5. THE QUARTER LUT has a dedicated carry-out net to route the fast-carry signal to and from adjacent LUTs, which helps implement fast-counter functions in one programmable function unit (PFU). In addition, the CIN and COUT ports route fast-carry signal between adjacent PFUs.


Design comparison: 4-bit counters

(a) 4-bit counter using ``D'' type register
Feedback signals: 9
Combinatorial logic levels: 2

(b) 4-bit counter using ``T'' type register
Feedback signals: 6
Combinatorial logic levels: 1

(c) 4-bit counter using maximal length LFSR technique
Feedback signals: 2
Combinatorial logic levels: 1

6. THREE 4-BIT COUNTER DESIGNS require different numbers of feedback signals and combinatorial logic levels. A D-register-based version requires nine feedback signals and two combinatorial logic levels (a). The T-type-register counter features six feedback signals and one combinatorial logic level (b). And finally, the LFSR counter needs only two feedback signals and one combinatorial logic level (c).

state of the fourth bit must be combined to determine the next state of the fourth bit. Using a T-type register decreases that number by one *(Fig. 6b)*. But by taking the LFSR approach, a 4-bit counter employs only two feedback signals to the XNOR *(Fig. 6c)*.

The registers in most modern CPLDs can be configured as T registers. Typically, the registers and their input product terms form macrocells. Then the macrocells are usually grouped in some form of logical cluster. These clusters are necessary to overcome the physical limitations of the device's interconnection matrix. For 100% global routability, this matrix expands in proportion with the square of the number of inputs to the matrix.

PHYSICAL LIMIT

However, the physical limit on product terms and inputs into one of the PLD clusters in a CPLD puts a cap on how many binary-counter bits can be implemented in a given cluster. For instance, in one vendor's CPLD architecture, only 18 signals are input into a given logic block, including two from dedicated inputs. This restricts the length of any straightforward counter design to 16 bits. Such a limitation is easily overcome by adding a terminal-count register that's active when the terminal count of the block is reached (look-ahead carry technique). The terminal count is then used to enable subsequent count stages.

Adding the terminal count circuitry will increase the design's complexity, though, as well as reduce the number of logic elements available for the actual counter and other circuitry. Fortunately, due to the wide AND functions provided by the sum-of-products array, most CPLD-based counters can generate the next-state logic within one macrocell, thus attaining a count speed equal to or near the $1/t_{co}$ of the device. This accounts for the outstanding performance results obtained by CPLDs in the PREP benchmarks.

Counter design in FPGAs is complicated by narrow input functions into the logic elements and channeled routing resources (versus some subset of global interconnect in CPLDs). While FPGAs typically feature a much higher register count than CPLDs, the number of inputs into any logic block is significantly smaller. Each input into a CPLD macrocell is a product term, and each product term is the AND function of all needed signals or their complements. Each FPGA cell input represents a simple, individual input signal.

The only way to increase the width of the input function to a flip-flop in an FPGA is to cascade multiple logic elements in depth and/or width. This consumes many available routing and logic resources. Cascading in depth slows the design down because each additional logic level contributes not only the logic delay for

OUTPUTS TO USE FOR MAXIMUM-LENGTH LFSR COUNTERS

'n'	Bits to XNOR	'n'	Bits to XNOR
3	3,2	21	21,19
4	4,3	22	22,21
5	5,3	23	23,18
6	6,5	24	24,23,22,17
7	7,6	25	25,22
8	8,6,5,4	26	26,6,2,1
9	9,5	27	27,5,2,1
10	10,7	28	28,25
11	11,9	29	29,27
12	12,6,4,1	30	30,6,4,1
13	13,4,3,1	31	31,28
14	14,5,3,1	32	32,22,2,1
15	15,14	33	33,20
16	16,15,13,4	34	34,27,2,1
17	17,14	35	35,33
18	18,11	36	36,25
19	19,6,2,1	37	37,5,4,3,2,1
20	20,17	38	38,6,5,1
		39	39,35

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Chart I	Actel	Actel	Xilinx	Altera
Device	A1240A	A1240A-2	XC4005A-5	EPM7256-20
Capacity[1]	15.3	15.3	15.4	14.7
Performance[2]	36.3 MHz	48.4 MHz	35.0 MHz	45.3 MHz
Price[3]	$68.80	$96.30	$138.70	$214.25

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Chart II	Actel	AMD
Device	A1225A	22V10Q-25
# Devices	1	12
Total Icc Power[4]	10 mA	660 mA
Total Price[5]	$42.50	$ 77.16

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1. Average number of PREP instances, approximately 4000 gates or 20 PALCE22V10s. 2. PREP Derived Data-average internal operating frequency, in MHz. 3. 100 piece PQFP price quoted by authorized distributor, August/September 1993. 4. Typical Icc per device multiplied by number of devices. 5. Based on 100 piece PLCC price quoted by authorized distributor, August/September 1993. ACT, PLICE, Designer, and the Actel logo are trademarks or registered trademarks of Actel Corporation. PREP is a trademark of the Programmable Electronics Performance Corporation. All other brand or product names are property of their respective holders.

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that level, but also the block-to-block routing delay.

Given the constraints that engineers face, there are two other solutions to increase counter speed: pipelining (or look-ahead carry circuitry) and pulse swallowing prescaling. The first involves pipelining the counter's LSB, or a few LSBs, to the clock-enable inputs of subsequent stages. This setup results in a small, fast counter that enables the larger, slower counter (which exploits the fact that the more-significant bits change at a slower rate than the less-significant bits). For instance, if an LSB is clocked at 50 MHz and its output enables subsequent bits, the clock enable for these bits changes at 25 MHz. This effectively halves the clock frequency to subsequent stages, and allows more traditional ripple-carry methodology to be used in these stages.

This same philosophy accounts for the fact that both parallel and ripple enable inputs are found on such standard 74xx TTL functions as 74LS191 and 74ACT162 counter devices. The parallel enable reduces the effective clock frequency to the more-significant stages. At this reduced rate, several additional stages can be cascaded with the ripple-carry method using a total ripple propagation delay of less than the effective clock period to these stages.

As a side note, consider the 4-bit PFU architecture of the ORCA device. The built-in fast carry circuitry allows simple 4-bit counters to run at nearly the rated speed of the device. Using a similar combined fast-parallel, slow-ripple count enable method can yield relatively large, fast counters in these devices.

However, pipelining doesn't resolve one critical problem with binary counters. That is, each successive bit needs to know the state of all preceding bits to decide whether or not to toggle. Consequently, the pipelining technique consumes considerable logic and routing, resulting in an unoptimized design from a density standpoint.

The pulse-swallowing prescaler technique is similar. A small, fast counter is used in front of a larger, slower counter. The small counter extends its count by one upon command by dividing either by N or N+1. Two examples are divide by 8/9 and divide by 128/129. The lower number is a power of two, and the second number is a power of 2, plus one. In a frequency-divider or synthesis application, engineers can use this fast counter. The counter swallows an additional pulse on command to generate any desired divide ratio. That way, engineers can fine-tune the overall counter chain to produce the required divide ratio.

This technique can be performed internally or externally with an FPGA. If done externally, there are available devices in the gigahertz range for high speeds. Internally, engineers are limited to the FPGA's traditional speed.

Externally, the pulse-swallowing prescaler technique incurs high device expense and added board space. There's also an extra flip-flop required for the N+1 condition, or for storing the swallowed pulse. The flip-flop exists only to provide that one extra state. It's not integral to the counter chain, but an extra flip-flop is needed for pulse swallowing.

In addition, there are certain unattainable divide ratios. This can be proven empirically by drawing the circuit and trying it. For example, a divide by 8/9 prescaler can't divide by certain numbers below 56. With a binary counter, on the other hand, engineers can look for *any* given pattern, decode it, reset the counter, and have a modulo-N counter with no problem. The LFSR version is slightly less straightforward—the output bit pattern for the selected length must be calculated before the decode/reset circuit can be designed. The utility program on the aforementioned AT&T FPGA Bulletin Board can assist in determining the required output pattern.☐

Bob Klein, a member of the technical staff at AT&T Bell Laboratories, holds an BSEE from Pennsylvania State University, Harrisburg.

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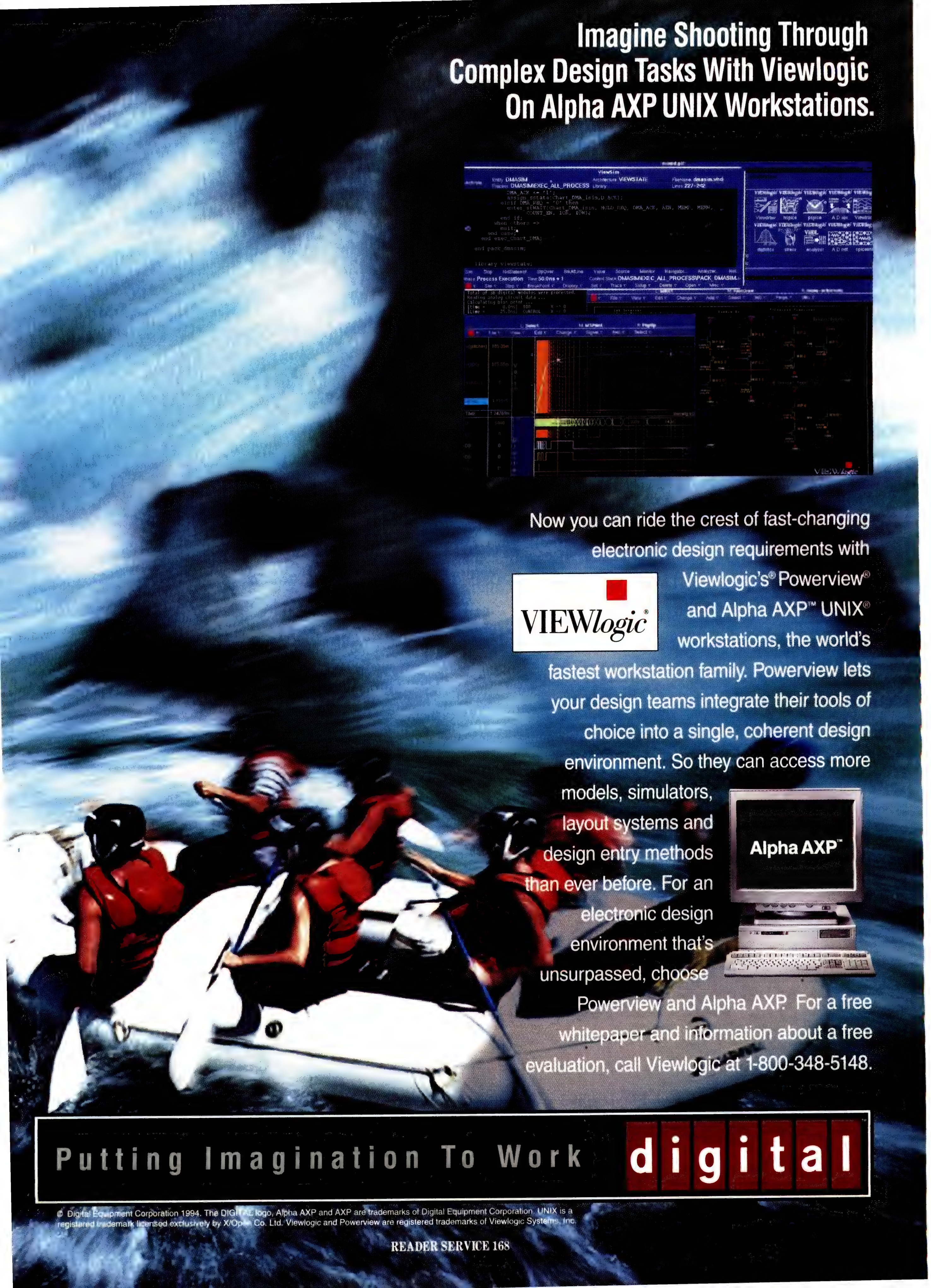

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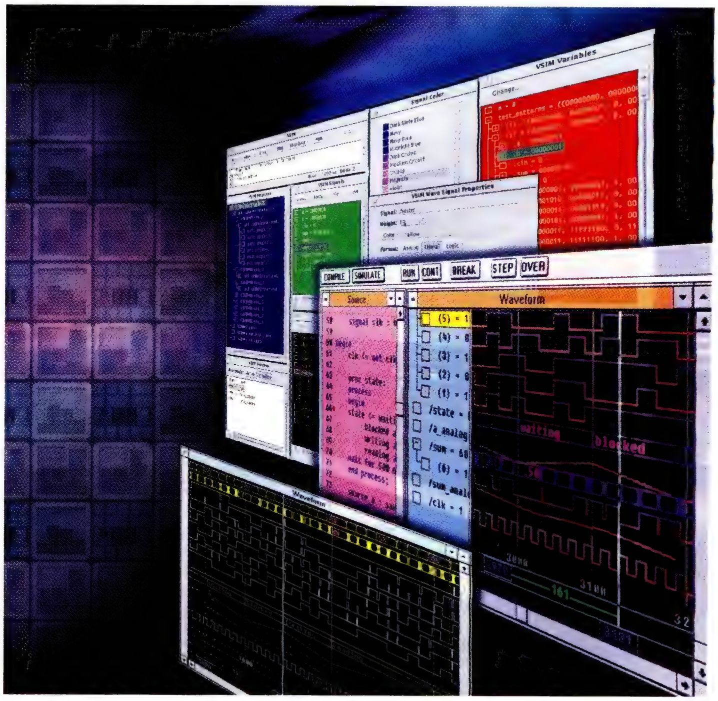

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CIRCLE 521

NOISE-IMMUNE DATA TRANSCEIVER

SAM OCHI

IXYS Corp., 3540 Bassett St., Santa Clara, CA 95054.

Sending and receiving digital control and status signals across electrically noisy (both EMI and RFI) grounds sometimes requires common-mode noise-rejection capability beyond that offered by the best optocouplers. One popular example of this involves the outputs of pulse-width-modulated inverters in high-power variable-speed ac motor drives. Its attendant noise transients climb as high as ±100 V/ns and voltage swings are 1200 V. The inverter output, prior to any EMI or RFI filtering, typically is the most convenient and information-rich point where high-speed current, voltage, and temperature sensors may be located. The best optocouplers usually are specified with only ±15 V/ns of common-mode noise capability, approximately 1/6th of the expected transients.

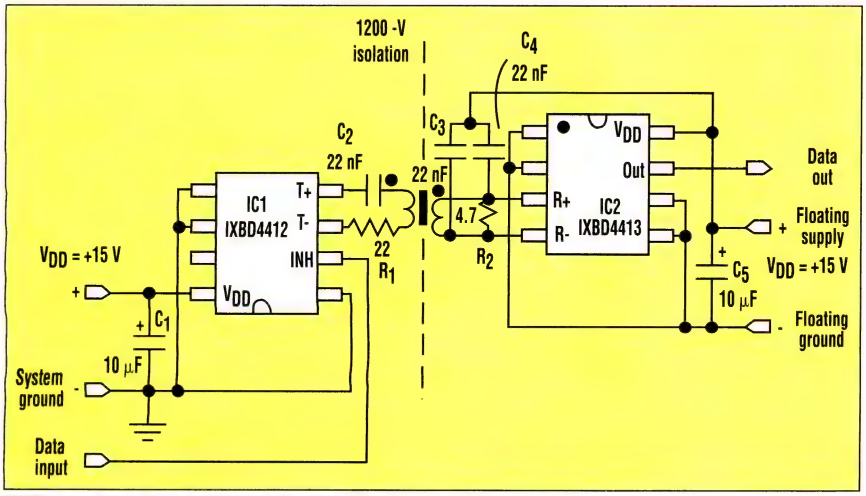
This circuit *(see the figure)* can fill that void: it's been tested error-free within ambient common-mode transients of ±100 V/ns at data rates to 3 Mbaud. Three techniques are used for good noise immunity. First, the communications signal transformer (T1) is segment-wound to minimize primary to secondary interwinding capacitance. Second, receiver input impedances are kept low to reduce sensitivity to coupled noise (4.7 Ω across the receiver inputs), and 22-nF capacitors shunt each receiver input to V_{DD}. Third, the receiver inputs respond to signals above 250 mV p-p because of the built-in 250-mV input hysteresis thresholds.

The transmitter (IC1), an IXBD4412, converts a 5-V CMOS or TTL signal at its INH (pin 2) to full 0-to-V_{DD} (+15 V) complementary output signals: T+ at pin 4 and T– at pin 3. The T+ and T– outputs are applied to T1's primary through R_1 and C_2. R_1 serves to limit the peak currents, while C_2 acts as a dc blocking capacitor. The secondary of T1 drives receiver inputs R+ (pin 3) and R– (pin 4) of the IXBD4413. The receiver's output is available at Out (pin 7), a 0 to V_{DD} output with up to ±2 A of current drive capability.

Low-noise, analog-circuit-layout techniques must be employed to minimize radiated noise pickup. The transmitter outputs of IC1 should be placed next to each other so that any radiation from each of the T+ or T– outputs are cancelled. The IC2 receiver inputs are run symmetrically and next to each other, with the distance from T1 being as short as is physically possible.

T1 is one-half of a dual transformer, with a primary to secondary turns ratio of 1:3. T1 is available from Fil-Mag (part #23Z129, phone: 619-569-6577) or BH Electronics (part #500-1914, phone: 612-894-9590).

T1 can also be created from scratch by following three simple steps. First, obtain a shield bead from either Fair-Rite (part #2661000101, phone: 914-865-2055), Philips (part #56 590 65-4B, phone: 800-367-8083), or TDK (part #HF50BB3.5x3x1.3, phone: 408-437-9585). Second, create the primary on this shield bead by winding 6 turns of #36 magnet wire. Third, produce the secondary by winding 2 turns of #30 wire-wrap wire. The two windings must be wound separately and kept away from each other to minimize capacitive coupling.☐



A 3-MBAUD NOISE-IMMUNE DATA transceiver can be created by using three basic techniques: segment-winding the communications signal transformer to minimize interwinding capacitance; keeping receiver input impedances low to reduce sensitivity to coupled noise; and including 250-mV input hysteresis thresholds so that receiver inputs respond to signals above 250 mV p-p.

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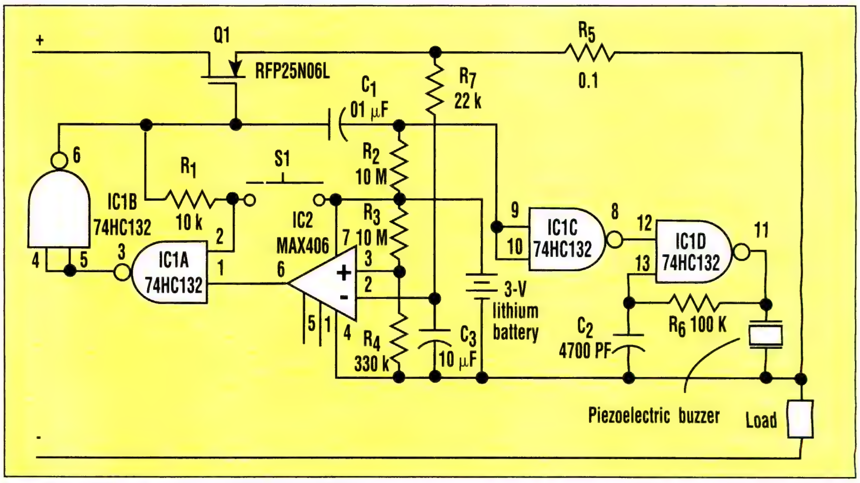
CIRCLE
522 FUSE SOUNDS OFF WHEN OVERLOADED

YONGPING XIA
EBT Inc., 23600 Telo Ave., Torrance, CA 90505.

Powered by a lithium battery, a self-powered solid-state fuse *(see the figure)* circuit that continuously measures the current running through it will cut off if the current is over 1 A, making a beeping sound for about 1 second. Because the circuit consumes only 1.2 µA of current in normal condition, a 100-mAh battery can run at least eight years.

A logic-level FET (Q1) is used as an on/off switch. The current through Q1 has a little drop voltage on R_5. This voltage compares with a constant voltage (0.1 V) provided by R_3 and R_4. If the current is more than 1 A, IC2's output will change from high to low. This change triggers a flip-flop formed by IC1A, IC1B, and R_1, so that IC1B's output becomes low. As a result, Q1 will turn off. High to low change on IC1B's output also generates a positive pulse (about 1 second) through C_1, R_2, and IC1C. This pulse allows IC1D, C_2, and R_6 to oscillate, which in turns drives a buzzer. To reset the circuit, S1 should be pushed to the point where IC1B returns to output high status.

The circuit uses a minuscule current. During the period when there's no beep, total current is only about 1.2 µA. Selecting a different R_5 or R_3R_4 ratio can change the fuse current setting. The maximum working voltage depends on Q1, which is 50 V if a RFP25N06L FET is used. The RFP25N06L can handle transient current up to 25 A. The response time of the fuse depends on R_7, C_3, and overload current.□



WHEN LOAD CURRENT is over 1 a, this solid-state fuse will beep for about 1 second, signaling an overload. When the circuit isn't beeping, it uses very little current—about 1.2 µA.

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CIRCLE
523 ONE-TRANSISTOR DIFFERENTIAL AMP

DAVID L. ALBEAN
Thomson Consumer Electronics, Corporate Research Americas,
600 N. Sherman Dr., Indianapolis, IN 46201-2598.

A differential amplifier can be easily implemented with a one-transistor circuit, a combined common-emitter/common-base connection.*(see the figure, a).*

With the transistor biased at about 1 mA of collector current, gain expressions can be derived using superposition:

- The ac output voltage is of the form:
$V_{out} = K_A V_A + K_B V_B$

- The gain experienced by V_A is that of a common-emitter stage:
$K_A = -R_3/(R_4 || R_5)$

- The gain experienced by V_B is that of a common-base stage:
$K_B = +(R_3/R_5)$

Note that the gains are of opposite sign. By choosing the magnitudes of K_A and K_B to be equal:
$V_{out} = K(V_B - V_A)$ where $K = (R_3/R_5)$
For K_A and K_B to be equal:
$(R_4 || R_5) \approx R_5$ (requires $R_4 >> R_5$)

It's evident that this circuit can implement $K_A >> K_B$ by setting $R_4 << R_5$. For example, setting $K_A = 5$ and $K_B = 1$ allows easy realization of a function like $V_{out} = (V_B - 5V_A)$.

If very accurate subtraction is required, add resistor R_A as a gain trim for K_A. R_A will act as a voltage divider with the bias network $(R_1 || R_2)$ to reduce the magnitude of value of K_A. This will allow K_A to be trimmed to match exactly the value of K_B.

Overall gain can be scaled via R_3.

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100-1500MHz	1.1	1.9	1.1	1.7
1500-3000MHz	1.8	2.7	1.8	2.5
Isolation(dB)	typ.	min.	typ.	min.
10-100MHz	60	40	60	40
100-1500MHz	40	28	40	30
1500-3000MHz	35	22	35	22
1dB Compression(dBm)	typ.	min.	typ.	min.
10-100MHz	17	6	17	6
100-1500MHz	27	19	27	19
1500-3000MHz	30	28	30	28
VSWR(ON)	typ. 1.3	max. 1.6	typ. 1.3	max. 1.6
Switching Time (μsec) (from 50% TTL to 90% RF)	typ. 2.0	max. 4.0	typ. 2.0	max. 4.0
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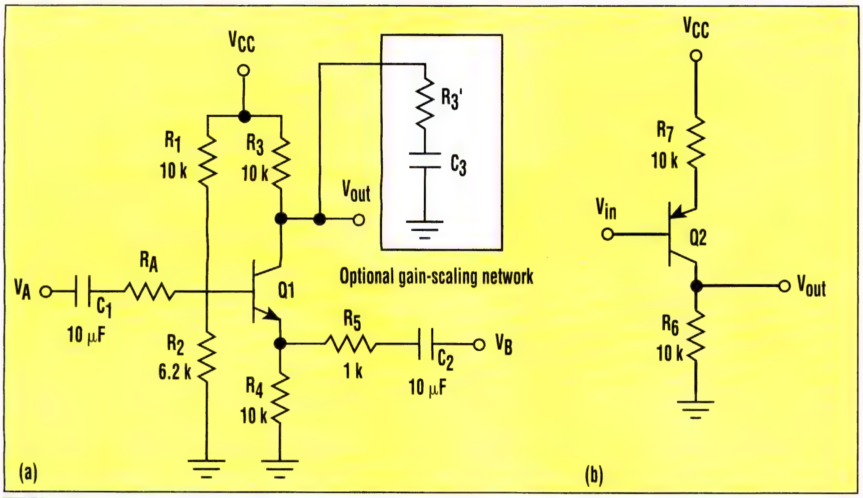

THIS DIFFERENTIAL AMPLIFIER (a) uses only one transistor in a combined common emitter/common base connection. As a power-supply rejection circuit, a pnp transistor is used (b).

If a lower gain is required, a series R/C combination should be used in parallel with R_3 to reduce the gain.

Looking more closely at the figure, the component values implement $V_{out} = 10(V_B - V_A)$; C_1 and C_2 are coupling capacitors; and R_1 and R_2 establish the dc bias and desired collector current. For $K = 1$, $V_{out} = (V_B - V_A)$, requires $R_3' = 1$ k.

This setup is also advantageous in a power-supply rejection circuit application *(see the figure, b)*. A pnp common emitter/common base circuit is employed.

The common-mode rejection of any ac ripple present on the V_{CC} line can be provided (due to imperfect bypassing), as long as the same ripple is present on its input (base). Again, the gains from the emitter and the base to the collector are equal but are opposite in sign.

The circuit probably is most useful in integrated circuit design, in which any remaining V_{CC} ripple can be cancelled by adding a stage of this type.☐

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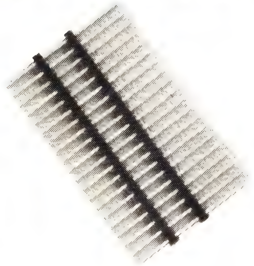

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New Generation Serial Nonvolatile Memories

The Missing Link for M68HC16 / MC68302 Designs: QSPI Serial Nonvolatile Memories

Migrating in the Motorola microcontroller family beyond the M68HC11 presents a problem for those applications which require non-volatile memory since the advanced 16 and 32 bit microcontrollers do not feature integrated E^{2}PROM. Xicor's full line of QSPI serial memories fills the void present in the M68HC16/68302 architecture. These serial devices are fully compatible with the QSPI port on the M68HC16 and operate at speeds up to 1MHz. The QSPI interface reduces the software overhead of the serial communication by handling much of the supervision in the interface itself rather than through software intervention.

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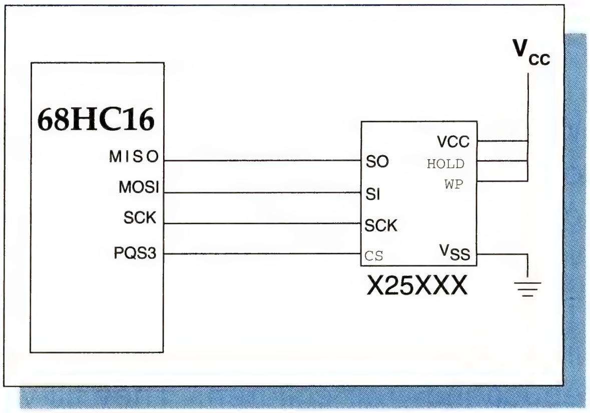

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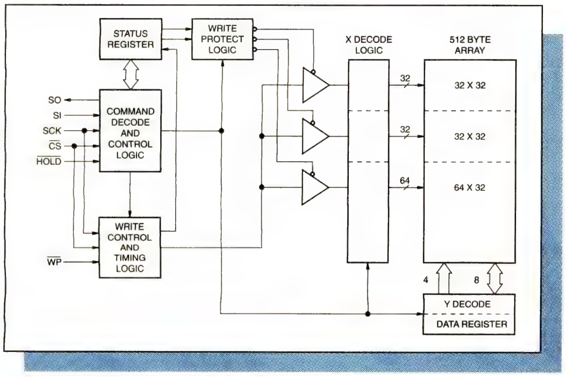

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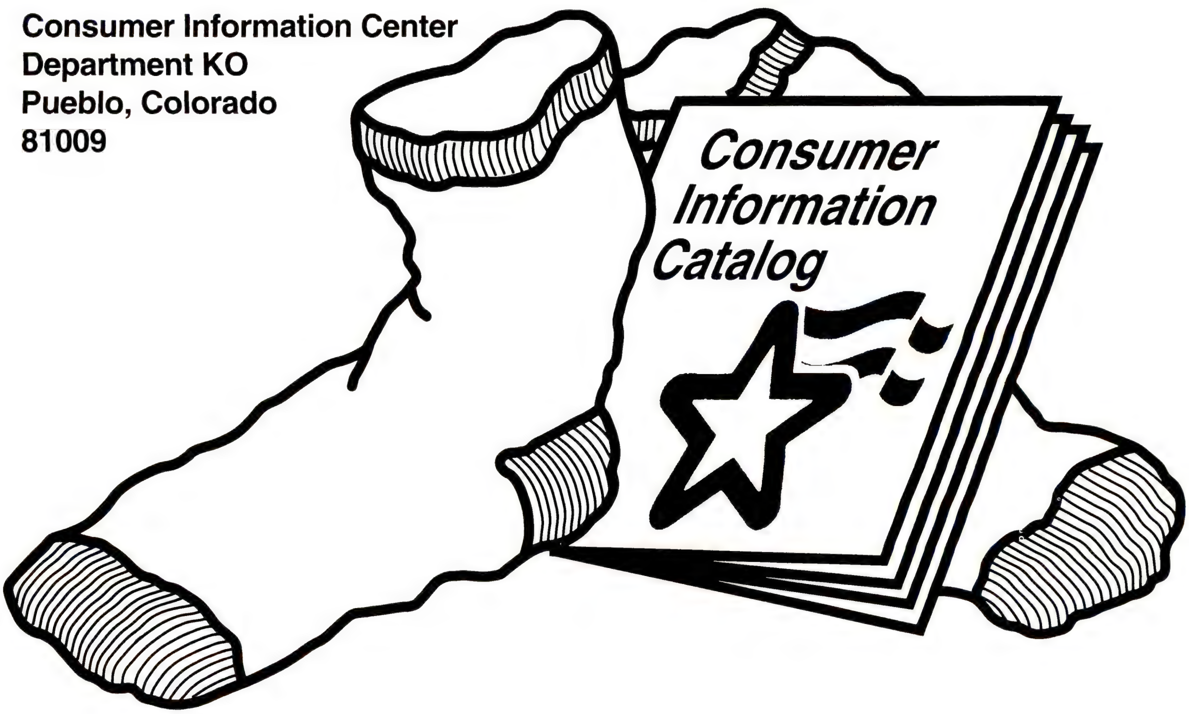

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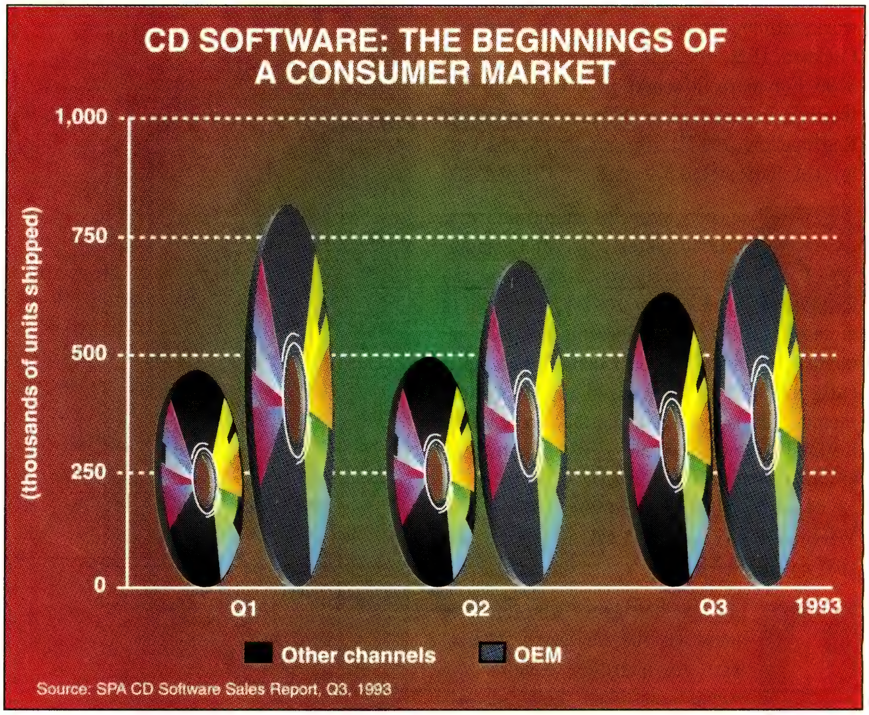
ELECTRONIC DESIGN

QUICK LOOK

EDITED BY SHERRIE VAN TYLE

MARKET FACTS

Software on compact disk (CD), one of the industry's fastest growing segments, racked up $97.1 million in revenues in the first three quarters of last year, according to a report by the Software Publishers Association. Based on data from 53 leading software companies in the CD market, 3.86 million software CDs were shipped, with 59% reaching the user from the original equipment manufacturer (OEM) while the rest were distributed through other channels. OEM unit sales remained fairly steady at about 750,000 units per quarter through 1993 *(see the figure)* while sales through distributors, direct sales, and so forth increased from 500,000 in the first and second quarters to about 635,000 in the third quarter. The third quarter data points to development of a viable consumer market for CD software, says David Tremblay, the association's research director, (202) 452-1600, ext. 317.



Source: SPA CD Software Sales Report, Q3, 1993

TALES FROM A SKUNK WORKS

Developing winning products in today's world is a difficult task. Companies that win keep an intense focus on delivering endless streams of innovative products to ensure their business success. Some good examples are Intel, Microsoft, and Hewlett-Packard. I cherish Andy Grove's saying, "Only the paranoid survive." This is war. Only if your upper management is paranoid about the dangers of falling behind are you likely to approach new product development with the needed focus, vigor, and sustained investment. Starting a successful skunk works requires support from the very top level of management.

Most firms lack this level of commitment. In a few leading firms the CEOs focus intensely on new products, but most have other priorities. Today's technology product markets are very unforgiving, and even the best players wind up with bruises and scars. The victors relentlessly drive weak firms away from new product capability. For example, former champions Wang and Control Data have essentially abandoned products, becoming system integrators and service companies. Others like them have been acquired. The Japanese call this practice *kudoka* (hollowing) and resist it strongly.

So the first task is education. If you want to do products today, you had better plan to win. Your firm needs to develop a shared vision of who is winning and losing in technology-based business, and what practices are working. Usually this means you need to tap outside viewpoints, collect much data, and convert it to shared knowledge. Your first task is to convince management that they can and must win at new products. One barrier is that managers are overloaded and drowning in data, but starved for knowledge. That's why consultants like me offer lectures and newsletters. We spend a lot of time filtering data and keeping up with trends. A workshop on new product development can help you get started.

Another promising development is a new Master's degree program, Management *in* Science and Technology. This integrated program consists of classes in finance, marketing, technology, and business. The focus is on teams who conquer growth markets through technology. Finally, the many good books on product development, shifts in corporate culture, and changes in the global economy include Peter Senge's *The Fifth Discipline*, Lester Thurow's *Head to Head*, Stephen Covey's *7 Habits of Highly Effective People*, and Clyde Prestowitz's *Trading Places*. Don't forget my own *High Tech With Low Risk* and *Engines of Prosperity* (due later this year). Stay in these learning loops until there is a shared vision and top-level support for sweeping change. Then start your skunk works.

John D. Trudel lectures and provides business development consulting: The Trudel Group, 52001 Columbia River Hwy., Scappoose, OR 97056; (503) 640-5599; fax 543-6361; e-mail: JohnTrudel@aol.com.

HOT PC PRODUCTS

XALT Office time management and communication software is intended for engineers and engineering workgroups who want to schedule individual and group meetings, events, daily tasks, and information. Besides client/server architecture, it has a graphical user interface, calendar view, permissions control, and e-mail. XALT office runs on Unix workstations, including those from Hewlett-Packard, IBM, and Sun. Single-user price is $199. For more information or a free 30-day trial via Internet, contact Thuridon Software Engineering, 269 Mt. Hermon Rd., Scotts Valley, CA 95066; (800) 872-9258. CIRCLE 460

Concern over PC manufacturers' shift to systems that don't implement parity checking led to the RAMexam utility. It detects memory failures by checking specific sequences of bit patterns. It installs automatically and can be configured to test system memory daily, weekly, monthly, or another defined frequency. The utility's automatic setup is compatible with DOS 6 MultiConfig. List price is $29.95. Contact Qualitas Inc., 7101 Wisconsin Ave., Suite 1386, Bethesda, MD 20814; (310) 907-6700. CIRCLE 461

Aimed at engineers who log long hours on the keyboard, MouseMitt Keyboarders cushion the carpal bones when the wrist rests on a work surface. The additional fabric and padding give extra warmth to the wrist and back of the hand, which helps to reduce strain on the tendons that work the fingers. Suggested list price is $19.95 a pair; $10.95, single. Contact MouseMitt International, 75 Green Valley Rd., Scotts Valley, CA 95066; (408) 335-9599. CIRCLE 462

The Dauphin DTR-1 mobile computer doubles as a pen-based system. The 486-based unit weighs 2.5 pounds and has dimensions of 9 by 5.5 by 1.25 in. It has note taking, sketching, and organizing functions. A detachable keyboard and I/O ports enable the unit to work as a subnotebook or the center of a desktop system. The Dauphin has up to 6 Mbytes of RAM, more than 75 Mbytes of hard disk storage (compressed), built-in fax/modem, a VGA backlit display, and optional internal Ethernet. It ships with DOS, Windows, and Windows for Pen Computing. Contact Dauphin Technology Inc., 377 E. Butterfield Rd., Suite 900, Lombard, IL 60148; (708) 971-3400; fax -8443. CIRCLE 463

KMET'S KORNER

...Perspectives on Time-to-Market

BY RON KMETOVICZ
President, Time to Market Associates Inc.
P. O. Box 443, 100 Prickly Pear Rd., Verdi, NV 89439; (702) 345-1455; fax (702) 345-0804

What does the typical new product development database look like? I'll answer this question from wisdom gained from years of observation. A new product has been defined and a cross-functional team, small in the early stages of development, begins doing the work necessary for forward progress. Verbal communication between team members guides forward progress with the help of materials (drawings, sketches, data tables, graphs, reports, screen images, prototypes, simulations, and the like) to arrive at some point of common understanding. As the image of the present situation forms, group discussions take place to make sense of the observations and decide on a course of action. These group discussions, or meetings, take place regularly; a schedule materializes. The schedule will be reviewed and adjusted. Observation, interaction, decision making, and schedule adjustment recurs until the work is done.

Engineers interact with one another on technical issues. They get involved exploring various approaches. Alternatives may be simulated or prototyped. Data from these exercises is recorded and analyzed. Usually, interactions take place after the evaluation to discuss the results; from the data comes a decision to take specific action on future work. While most of the engineers focus on the most quantifiable work, some get involved with their marketing counterparts on "fuzzier" issues. Here, attempts are made to correctly align product cost, performance, features, and development time to effectively respond to the market. Some data, some experimentation (in the form of focus groups), and leadership gut-feel resolves conflict and produces decisions. Manufacturing has its voice too—engineering and marketing actions directly affect materials, assembly, test, and distribution. As such, these inputs become an integral part of the scheduling process.

While all of the cross-functional interaction takes place, timing estimates are produced. Where did this timeline come from? It's usually from someone who attempts to integrate all the intangible information in circulation throughout the organization. Somehow, from this abundance of slightly correlated data, a person, usually a project or program manager, steps forward and produces a schedule using the human skills of observation, interpretation, association, discussion, and inference. The schedule becomes a mind game shared between its originator and the affected participants—the database exists in the minds of the new product development team. To support what the mind knows and some of those single page detailed calculations to forecast the "ship" date, a summary of the timeline then gets entered into a project-management software tool.

The tool serves to encourage the distribution of scheduling information through colorful charts and some simple reports. As time passes, comparison of actual completion dates to forecasted completion dates becomes possible. Then the tool serves to show if progress is ahead of, or behind, schedule. Sometimes this level of project tracking works through intermediate progress checkpoints all the way to the end; but most of the time it fails to show anything more than the obvious of always being late. If something is going wrong, or is about to go wrong, there is no way to detect it in the data—the tool does nothing to identify problems. Problem identification and reporting happens verbally or by written report. It's up to the collective "project brain" to figure out what to do with them. When the next actions are identified, a new schedule is created and these dates are entered into the system.

Under this situation, meeting time-to-market challenges becomes a bit difficult. Where do you get the data needed to make trade-off decisions between resources, functionality, performance, money, and time under a brain-based database? Well, you call a meeting . . .

"It's About Time!" a workshop of new-product development organization will be held at Santa Clara University's Executive Development Center on April 7, 1994. Call John Blumenson, the center's assistant director at (408) 554-4521; fax -5143.

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TRANSFERS
MEASURES
PLACES
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READER SERVICE 175

...About customer delight

BY FRANK J. BURGE
Director of Market Development for Electronic Design

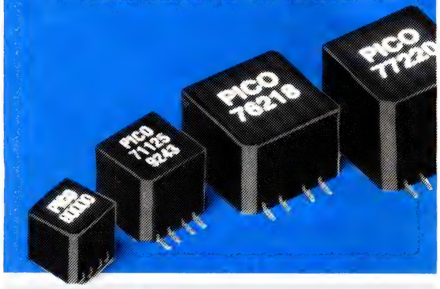
Delighting customers is today's strategy for survival. Automakers are on a campaign to make buying a car a haggle-free experience. Just about every time I turn on the TV, there's an ad from an auto company about value pricing. The pitch is that all the options are bundled into one low sticker price. It's implied that the sticker price is the best price you'll get, so there's no need to haggle. I give the auto companies good marks for making it more comfortable for me to buy, and hopefully the no-haggling, bundling strategy will win them new friends and extra sales. Good for them.

But while the auto manufacturers are trying to polish their image with the customer, the Ford dealer in my town is doing just the opposite. Nutso. My wife has an old Mustang convertible and when the new Mustangs arrive, she suggests we drive over to the Ford dealer to have a look. Having been brainwashed by the value pricing, all options bundled into the sticker game, I look at the sticker price on the Mustang convertible. But what is that sticker next to the factory's suggested price? It's the dealer's sticker. Guess this Ford dealer figures if Ford has stickers so can the dealer. The only hitch is that the dealer's sticker has a $4,000 adder for the Mustang convertible.

That's right. If you want to buy that Mustang you pay the price suggested by the factory, plus the dealer's $4,000 adder. The gotcha sticker game. Now it may be that the dealer figures its salespeople will go soft with all this no-haggling, options bundled into one sticker price game. So to keep *them* in shape the dealer tacks on another $4,000 then lets the sales troops and the customers wrestle for the best deal. Just *like old* times. More fun too. But that dealer's policy has soured me on Ford. Even though I assume Ford had nothing to do with it.

A few days after the Ford episode I call my friend Tom's office to get the correct spelling of his last name. I want to send him an invitation to attend a marketing luncheon with me. Now I've known Tom for 20 years, but I have a tough time remembering the correct spelling of his last name. And I seldom write him so I don't get much practice remembering. Anyway when I call, I get the switchboard operator and ask him if he would be so kind as to spell Tom's last name. But before I can say anything else I am transferred to a person in the Human Relations Department who then begins to quiz me on why I want the spelling of Tom's last name. I explain but my explanation isn't good enough because the Human Relations idiot asks: "If you are a *friend*, how come you can't spell his last name?" I get miffed and point out that I may also be her company's largest customer. With that she hangs up. I then dial again and ask for Tom's office and get his secretary. She gives me the correct spelling of his name and does so with a smile.

Doing business in the "nanosecond nineties" is more competitive than it's ever been. Customers expect more because *their* customers expect more from them. And most companies have programs aimed at delighting customers. Ford has spent years and *zillions* of dollars to drive home Ford Quality and the implied quality of a relationship with Ford. Yet in a few minutes, everything they have worked so hard to build is destroyed by an over aggressive dealer. The same is true for my friend Tom's semiconductor company. Most of the people in his company *are responsive* to customer requests and are dedicated to customer satisfaction. Yet for me, all they have worked to *build* was destroyed because of the rude behavior of just one person in Human Relations who just doesn't get it. If there's a lesson in all this, it's that we all have ownership in the process of delighting customers. Pass it on.



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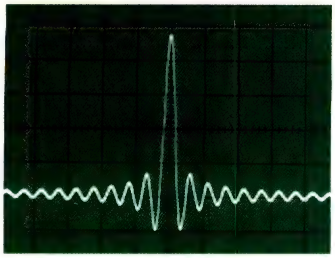

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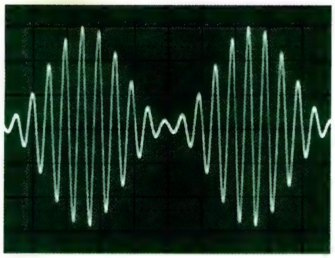

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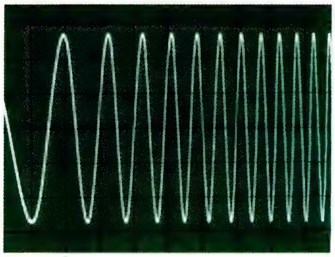

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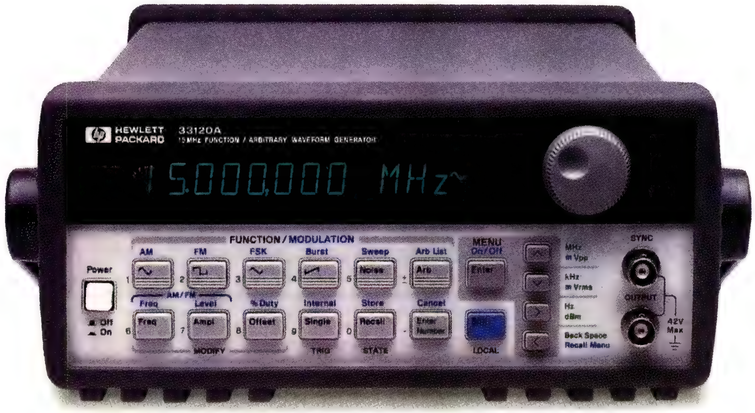

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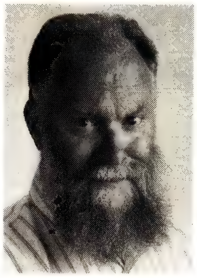

BOB'S MAILBOX

Dear Bob:

I really enjoy your pokes at Taguchi and Fuzzy Logic. To further emphasize how out-of-touch our engineering academics have gotten, I offer the following paragraphs for one of your "Mailbox" columns:

"Your critiques of Taguchi Optimization and Fuzzy Logic have been a great service to us engineering practitioners. Do not, however, interpret the dearth of practical applications to mean that these technologies have been less than successful. To the contrary, Taguchi's exuberant lectures to technologically defenseless managers about the hypothetical success of some ill-founded analytic hocus-pocus have certainly succeeded in putting high-priced bread on his table. With similar success, academics armed with Fuzzy Logic have transformed simple, low-gain, well-understood servo loops into esoterica, thereby hoodwinking the taxpayers out of $100K research grants.

More seriously, however, the failure of these promotions to produce the engineering efficiencies they tout points up a much more troubling problem than simple delusion. The academic community has become isolated from the engineering arts they profess to teach. I doubt that 1 in 50 American electrical-engineering professors could design a production-worthy product. They do not know what components and materials are available, what limitations and strengths these products have, what configurations and combinations are most practical, or what manufacturing efficiencies and problems their choices create. In short, all they know is mathematical analysis of idealized circuits—a very small part of the total design task.

Although they clearly lack the wisdom and knowledge essential for success in engineering, academics still wish the prestige of being considered industrial experts in the field their title professes. Just as medieval alchemists sought to concoct valuable gold from an incomplete understanding of chemistry, our modern university alchemists seek to concoct practical designs from an incomplete understanding of engineering. Having only analytic skills, the alchemists' naive and ill-targeted mathematical incantations serve as the modern mortar and pestle.

It is not that we don't appreciate the attempts of our monochromatic university brethren to shed light on the engineering process, it's just that we wish they would have more respect for the complexity of the total design problem."

There, Bob, now how's that for self-control and diplomacy?

JAMES A. KUZDRALL, P.E.
President
Intrel Service Co.
Nashua, N.H.

James, I think that most EE professors can contribute good stuff to a project team—just as most engineers in industry can—even though they are not all good at running the whole project.—RAP

Good Morning Bob,

...I don't think I ever told you about truck 2 (T2). I have encountered various mysteries in electronic equipment, usually small deviations from ideal behavior. I haven't solved every mystery, but usually I have a notion of the cause, such as nonlinearity, or noise or drift, or parasitic L, R, or C. But nothing that needed a magical explanation. That is, except good old T2.

I spent 1974 at McMurdo station, Antarctica. During the summer there are various trucks in the motor pool, but during the winter when there are only 3 permanent experiments, (riometers, cosmic ray counters, and satellite tracking) we had assigned trucks. My predecessors gave me a few tips (they laughed all the way to the plane), but they were most emphatic that I should insist on T2 during the winter.

That was good advice. I was able to start it even on the coldest days. I had to do without T2 for awhile, because one morning when there were only two vehicles moving in the base (my partner in T2 and a fork lift), they tried to occupy the same space at the same time. But we had a good mechanic, an ex-linebacker from USC, who intimidated T2 back into service. This was really fortunate.

I got to McMurdo just before the base was isolated for the winter. When summer came again, about 7 months later, and T2 was back in the motor pool, the guy running the riometer (two dipole antennas that measure RF noise from the sky at various frequencies in the 2-to-40 MHz bands) had been there a full year. He convinced the folks in charge and me that I could look after the riometer for a week while he took R&R in New Zealand (nearest civilization with an airport). He never came back.

Well, the old riometer was automated with relays and RTL logic. Every few minutes it scanned the frequencies and recorded the levels in a multipoint recorder, which was a wondrous mechanical thing that could make marks on chart paper with about 12 different colors. When things worked fine, there would be 12 smoothly varying curves on the chart.

I soon found out that things worked fine for about 30 hours at a stretch. After that, the multipoint recorder started scattering colored marks all over the chart. I never found out what was wrong, because in the process of opening panels and disconnecting cables to get into the thing, it would start working.

It was frustrating. The riometer was away from the base behind a hill to cut down on RF noise coming from the base, so I had to drive a truck out there. Sometimes, the riometer would start working just as I drove up. I could tell by looking at the chart when it had stopped working right and when it started.

Then I noticed an amazing thing. Every time I drove up to the riometer in T2, it started working. No other truck had this effect. After verifying this, I finagled T2 once a day and drove up to the riometer. It worked fine for the rest of my tour. I never did reveal to anyone why I was so insistent on driving T2. Sometimes the bureaucrats wouldn't give me T2, but I had a duplicate set of keys and just took it during the night.

There aren't many trucks that know how to make electronic equipment work. I suppose that T2 had really big ignition noise that somehow reset whatever was going nuts in the riometer, but magic is just as good an explanation.

ROY McCAMMON
3M Test and Measurement Systems
Austin, Texas

Roy, when you are troubleshooting an intermittent problem, an ability to chase away the problem is not necessarily more valuable that the ability to restart the trouble. Right?—RAP

Dear Bob:

I just received the February 7 issue of Electronic Design, and read your column on the relevance of Deming's stand on inspection to the integrated circuit business. Deming has stated explicitly his view of inspection in this field. I quote from page 29 of his book "*Out of the Crises*," published in 1986 by MIT: "We must note that there are exceptions, circumstances in which mistakes and duds are inevitable but intolerable. An example is, I believe, manufacture of complicated integrated circuits. Separation of good ones from bad ones is the only way out. Calculations and other paperwork in a bank or an insurance company is another example. It is important to carry out inspection at the right point for minimum total cost."

ARTHUR DAVIDSON
Senior Engineer
Westinghouse STC
Pittsburgh, Pa.

Mr. Deming's index said to look for "integrated circuits" on page 31. Those comments were not on page 31, but seem to have turned up later on page 29. Now, what is the explicit definition of a "complicated" IC? A quad op amp but not a 741? A dual flip-flop but not a quad gate? Would YOU like to buy op amps, gates, or transistors that have not been tested? Impossible—nobody will sell you one.—RAP

REUNION STUFF

All Alumni, Alumnae, and Survivors of (Teledyne) Philbrick Researches, plan for a Reunion at 5 P.M., April 20, at the Hilton Inn across from the Philbrick plant, Allied Dr., Dedham, Mass. For details, contact Cruise Director Joe LoSciuto, 510 Grove St., Norwell, MA 02061; (617) 659-4423. If you can't attend, send a letter to Joe. Keep the faith!—RAP

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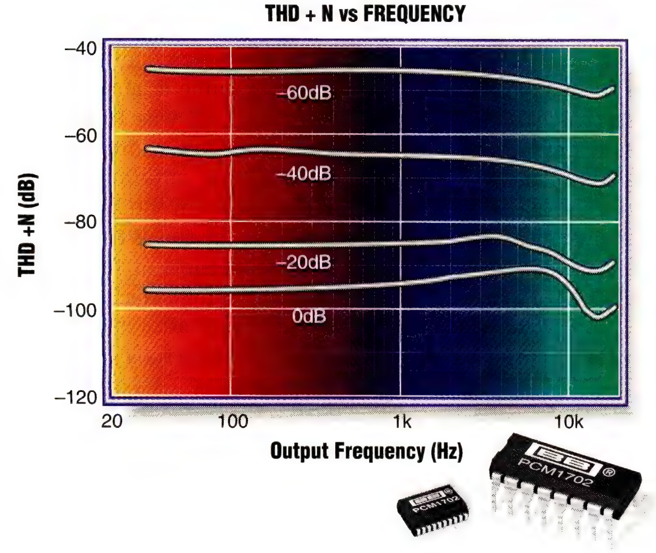

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ELECTRONIC DESIGN

SMT LEDs Fill The Bill For Right-Angle Viewing

There's more than one way to bring light from the LED to the viewer.

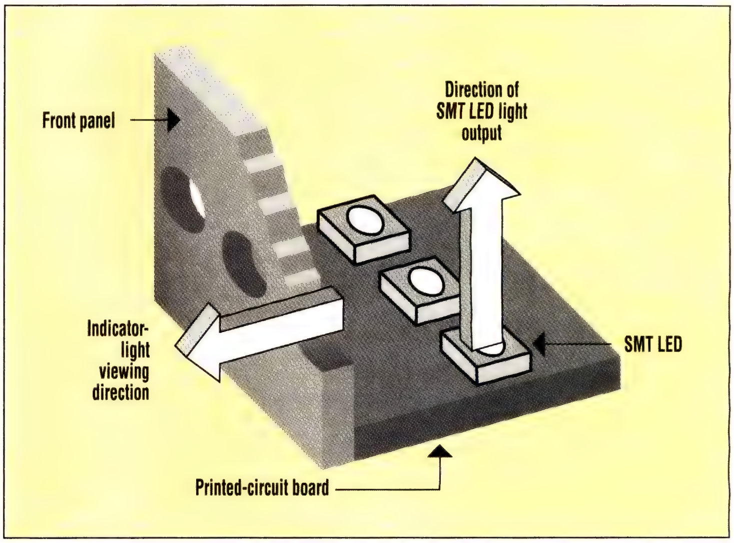
BY RAND EIKELBERGER AND JOE HURLEY

Dialight Corp., 1913 Atlantic Ave., Manasquan, NJ 08736; (908) 223-9400.

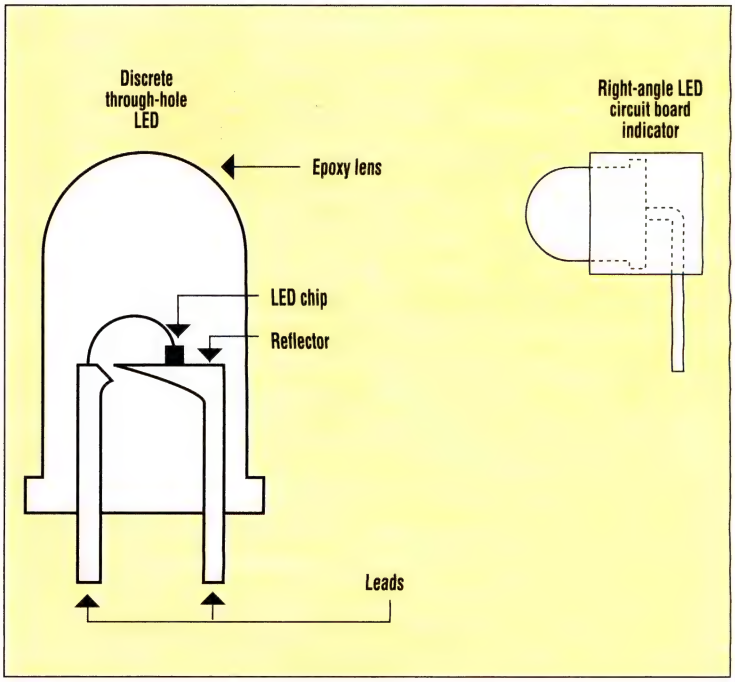
Although surface-mount technology (SMT) is applicable to a majority of electronic components, the most common means of mounting light-emitting diodes (LEDs) remains wave soldering. However, the demand to eliminate mixed technologies on the circuit board and for exclusive use of SMT continues to intensify. Doing so would enable manufacturers to achieve greater production economies.

The SMT LED emits light in a direction perpendicular to the circuit board, yet the desired viewing direction of the indicator is often parallel to the board *(Fig. 1)*. Consequently, the goals of LED-indicator manufacturers are two-fold: To combine SMT compatibility with the traditional performance designers have come to rely on in through-hole LEDs, and to efficiently and cost-effectively transmit the light in a right angle from the device to the user in an aesthetically pleasing fashion.

In attempting to translate through-hole performance into an SMT implementation, designers often first choose the traditional cast epoxy through-hole package and adapt it to SMT. These devices are a proven indicator solution, are available in a bewildering array of shapes and sizes, and incorporate lenses that can protrude through a panel or be used to backlight a front-panel legend.


Front panel
Direction of SMT LED light output
Indicator-light viewing direction
SMT LED
Printed-circuit board

1. The SMT LED emits light in a direction perpendicular to the circuit board, yet the desired viewing direction of the indicator is often parallel to the board.


Discrete through-hole LED
Epoxy lens
LED chip
Reflector
Leads
Right-angle LED circuit board indicator

2. Several failure modes exist with conventional cast-epoxy through-hole LED indicators, thus making the devices unsuitable for SMT processing. For instance, the reflow process can soften the lens epoxy enough that the stresses move the leads and break the bond wire to the LED chip.

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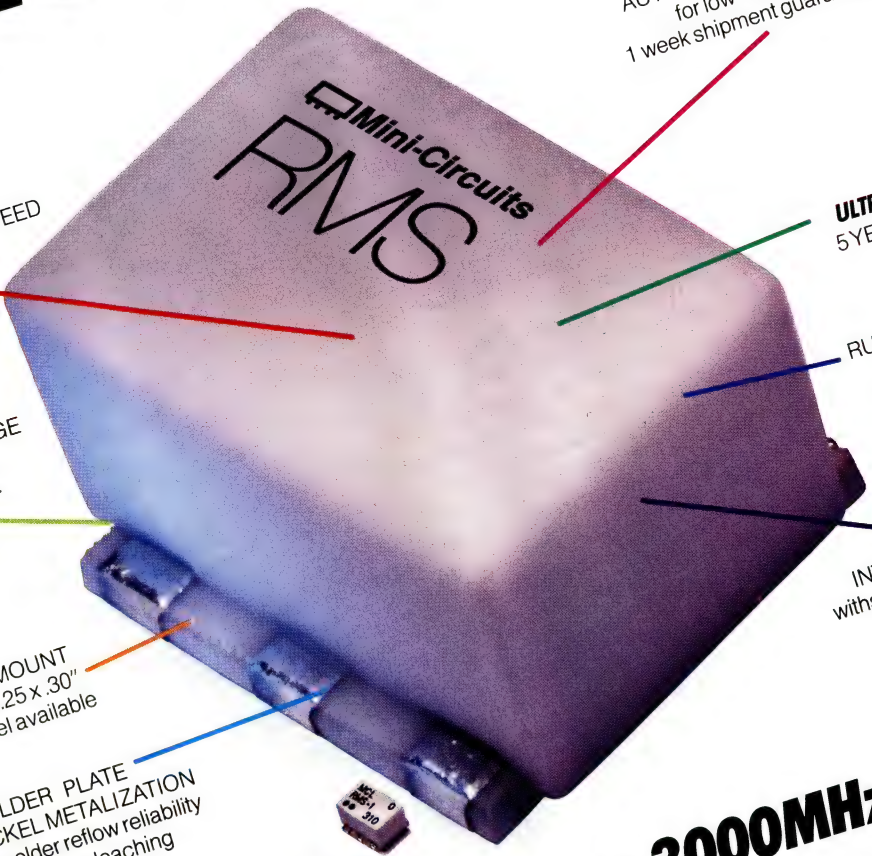

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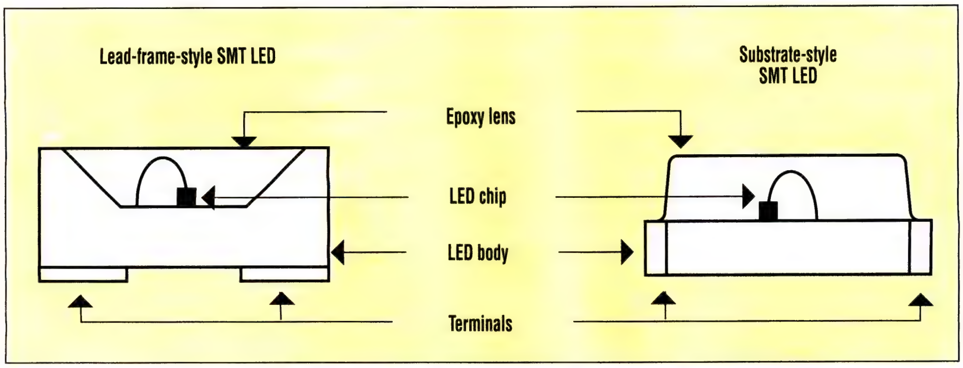


3. Two types of SMT-compatible LEDs are available: leadframe and substrate-style.

However, cast-epoxy through-hole LEDs aren't the solution of choice in SMT applications because they generally are incompatible with the SMT process.

Cast-epoxy through-hole LEDs consist of two leads—one with a coined reflector on which the LED die is attached with conductive epoxy, and the other with the bond wire attached *(Fig. 2)*. The leads, die, and bonding wire are encased in a cast-epoxy lens that also acts as the body of the assembly. The typical right-angle pc-board indicator includes such an LED, inserted into a plastic housing with the leads bent for printed-circuit-board insertion. Devices of this nature also can be lead-formed to accommodate mounting them as surface-mounted components.

However, forming the leads of cast-epoxy LEDs to convert them for right-angle lighting often creates residual stresses. The reflow process may easily heat and soften the lens epoxy to the extent that these stresses move the leads and break the bond wire. Even if the leads are unstressed, the mismatched coefficients of thermal expansion within the LED may cause the bond wire to break.

Another failure mode lies in rapid heating of the component. Such heating vaporizes any moisture present in the component, creating eruptions that can cause delamination of the die from the substrate.

In short, cast-epoxy LEDs, although initially tempting to modify for SMT, frequently have proven unreliable. As a result, LEDs are being designed specifically to survive the SMT-soldering process.

SMT LED packages must be manufactured in a shape, size, and weight that makes them compatible with component packaging and delivery systems. They must be small enough to fit in EIA-standard tape-and-reel packaging, and their weight must be low enough not to hinder vacuum pick-up or cause the component to misalign during high-speed, pick-and-place nozzle movements.

It's also helpful if the component has a flat top so that a standard nozzle can develop adequate suction. The packages must be able to withstand the high reflow temperatures and solvents encountered in the SMT environment. In addition, the optics and aesthetic features of the devices must survive the process unscathed.

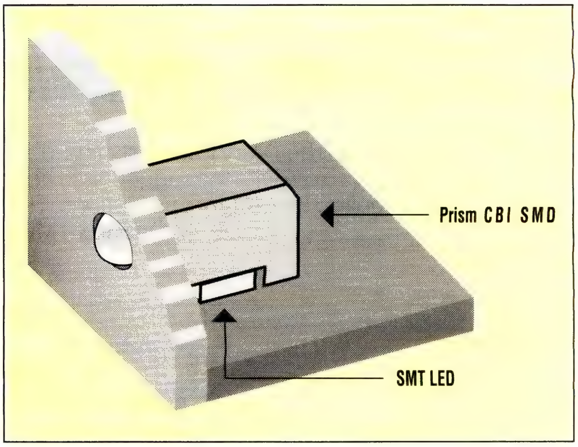
Unlike their through-hole counterparts, which incorporate secondary optics such as a reflector, lens, and diffuser within the device, SMT LEDs often require these features to be added externally, based on the needs of the application. Designers who opt for SMT LEDs must realize that the basic device is just a point source of light in a package designed for manufacturing compatibility. In addition, designers must address the issue of providing secondary optics.

For those considering SMT LEDs, two types of construction are available: substrate and leadframe *(Fig. 3)*. The substrate category itself offers two choices. The first is ceramic, such as the Dialight 597-7000 Series; the second is a glass-epoxy material. In either case, the LED die is bonded to terminals that are integrated into the substrate. In the leadframe package style, the leadframe is molded into a high-temperature plastic housing and the LED chip is bonded directly to the leadframe.

When adding secondary optics to the discrete SMT LED, designers are given two alternatives. The first is a complete, fully process-compatible component containing a light source and optics. It doesn't require post-process insertion of additional components on the circuit board. A good example of this approach is Dialight's Prism CBI Series device, which incorporates a surface-mounted SMT LED and a right-angle lensing system *(Fig. 4)*.

There's a limited choice of sizes and shapes with this approach, and a high-volume application is generally required to justify investment in a custom design. The devices also can't be used for a vertical column of indicators because they aren't stackable.

The second method of adding secondary optics is to place discrete SMT LEDs on the board and then attach a light pipe after the soldering process *(Fig. 5)*. The advantages of this approach include flexibility in the shapes and sizes that can be used, and better access to the SMT LED for rework and inspection. LED alignment is less critical with



4. The complete SMT-compatible right-angle indicator is one that requires no post-processing insertion of additional components on the pc board. Dialight's Prism CBI device is one such example.

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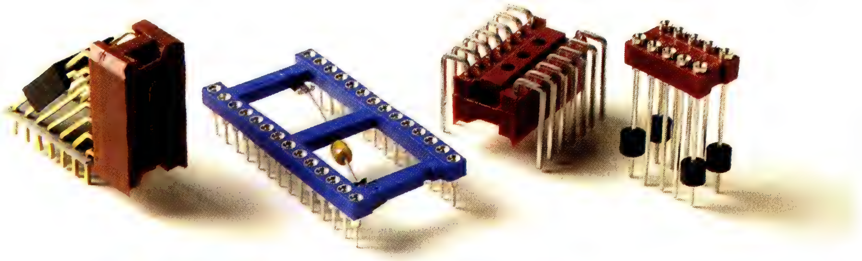

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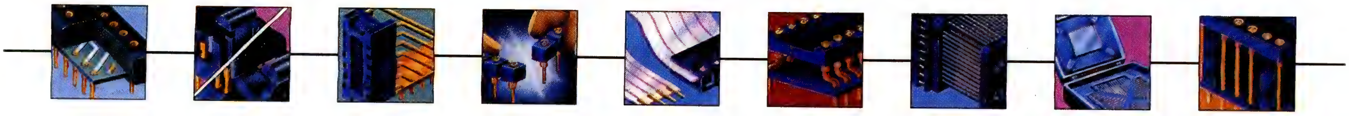

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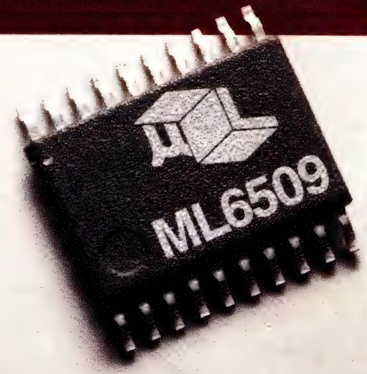

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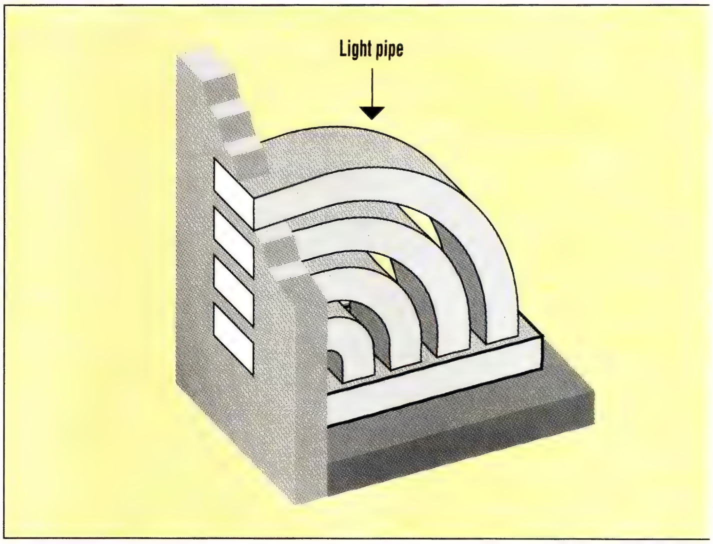

5. One means of transferring light from the pc-board-mounted LED to the outside world is through the light pipe. While this technique lends flexibility to the design process, it does require a secondary post-process operation. In this example, light is piped from four SMT LEDs to the front panel.

this approach as well.

In addition, depending on the complexity of the light pipe, the investment can be substantially less than the single-component solution just described. Its only significant limitation is that a post-process secondary operation is required to insert the light pipe into the board.

Light pipes are particularly useful in applications requiring an array of LED indicators. With careful light-pipe design, it's often possible to mold a single part to redirect the light from multiple LEDs to multiple front-panel indicator positions without optical crosstalk between them. This can result in a lower installed cost per indicator position.

From a cost standpoint, it sometimes appears less expensive to continue manufacturing mixed-technology circuit boards because the SMT component can be more expensive than its through-hole counterpar
However, the total installed co
usually is less when using
SMT indicator because it
much easier to install and mo
components can be placed
the board. In addition, the d
signer can use both sides of t
board. Making the move
SMT also reduces by one t
types of components that mu
still be through-hole mounte
expediting the conversion to
all-SMT assembly.

Fortunately for designers, t
number of LED indicator sol
tions available for SMT is pro
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choose the proper solution fo
given design.

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(CO) (ST) (MT) (TR)
CIRCLE 814

CTS
Frequency Controls Div.
400 Reimann Ave.
Sandwich, IL 60548
(815) 786-8411
(MC) (QC) (SC) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 815

CTS Corp.
Resistor Networks
406 Parr Rd.
Berne, IN 46711
(219) 589-3111
(TF) (RN)
CIRCLE 816

Caddock Electronics Inc.
Applied Sciences Div.
17271 N. Umpqua Hwy.
Roseburg, OR 97470
(503) 496-0700
(TF) (HR) (MO) (RN)
CIRCLE 817

California Micro Devices Corp.
215 Topaz St.
Milpitas, CA 95035
(408) 263-3214
(TH) (CH) (RN) (CP) (CN)
CIRCLE 818

Cesiwid Inc.
Globar Div.
P.O. Box 339
3425 Hyde Park Blvd.
Niagara Falls, NY 14302
(716) 278-2521
(CR)
CIRCLE 819

Champion Technologies Inc.
2553 N. Edgington St.
Franklin Park, IL 60131
(708) 451-1000
(CY) (TC) (VC) (CK) (SO)
CIRCLE 820

Clarostat Mfg. Co.
1600 W. Plano Pkwy.
Plano, TX 75075
(800) 448-2900
(CE) (WW) (CO) (ST) (MT)
(TR) (EM) (IE) (IS) (OS)
CIRCLE 821

Coilcraft Inc.
1102 Silverlake Rd.
Cary, IL 60013
(708) 639-2361
(IF) (RF) (SU) (PF)
CIRCLE 822

Coiltronics Inc.
6000 Park of Commerce Blvd.
Boca Raton, FL 33487
(407) 241-7876
(AF) (IF) (RF) (SU) (PF)
CIRCLE 823

Cornell-Dubilier
P.O. Box 128
538 Sangamo Rd.
Pickens, SC 29672
(803) 878-6311
(EA) (ED) (FL) (FP) (FY)
(MI) (CP) (SU)
CIRCLE 824

Curtis Industries
2400 S. 43rd St.
Milwaukee, WI 53219
(414) 649-4200
(PF)
CIRCLE 825

Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(310) 640-0442
(LL)
CIRCLE 826

Dialight Corp.
1913 Atlantic Ave.
Manasquan, NJ 08736
(908) 223-9400
(IE) (IS) (LL) (LI)
CIRCLE 827

Durel Corp.
645 W. 24th St.
Tempe, AZ 85282
(602) 731-6201
(UV)
CIRCLE 828

EBG Inc.
3705 Trindle Rd.
Camp Hill, PA 17011-4335
(717) 737-9877
(CR) (MN) (TF) (TH)
(HR) (MO) (RN)
CIRCLE 829

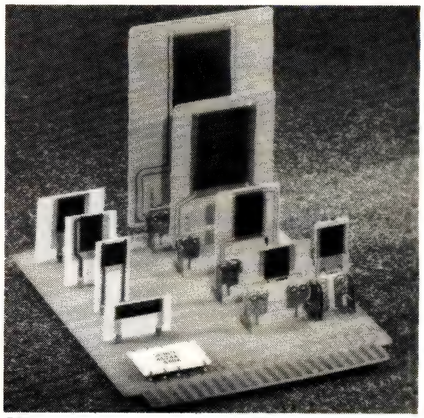
ESC Electronics Corp.
534 Bergen Blvd.
Palisades Park, NJ 07650
(201) 947-0400
(AF) (IF) (RF) (SU) (PL) (PF)
CIRCLE 830

Electrocube Inc.
1307 S. Myrtle Ave.
Monrovia, CA 91016
(818) 301-0122
(FL) (FP) (FY) (FT) (CN)
CIRCLE 831

(see p. 130 for key)

(continued on p. 127)

▼ RESISTOR RANGES EXPAND WATTAGES



New wattage ratings have been added to the PECOS and Power Chip resistor product lines. The PECOS (porcelain enamel coating on steel) products now include a 15-W version in addition to the 10-, 20-, 50-, and 100-W standard types. The 15-W size comes in standard tolerances of ±1 and 5% in values from 1 to 250 kΩ. The Power Chip series now offers a "side-saddle" configuration rated at 5 W. Pricing is $0.94 for the 15-W PECOS device and $0.31 for the Power Chip side-saddle 5-W unit. Both prices are for lots of 1000 with delivery in 10 to 12 weeks.

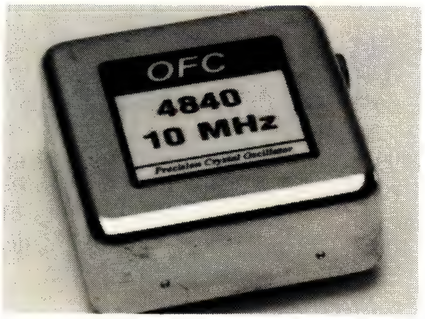
Ohmite Mfg. Co.
3601 W. Howard St.
Skokie, IL 60076
(708) 675-2600
▶ **CIRCLE 601**

▼ DIMPLED CONTACTS GUARD TIMING CRYSTAL

Dimpled SMT contacts that act as standoffs give the H-250 SMT crystal unit some needed pc-board clearance for better cleaning after soldering as well as decreased stress on the crystal blank during the soldering process itself. Applications for these quartz crystals include hard disk drives, cordless phones, TV tuners, video camcorders, and others. Frequency tolerances available for 25°C are ±10 ppm, ±30 ppm, ±50 ppm, and ±100 ppm. Frequency stability is as tight as ±2 ppm. Shunt capacitance is just 7 pF. Pricing is $1 in lots of 10,000. Delivery is in 4 to 6 weeks after receipt of order.

Raltron Electronics Corp.
2315 N.W. 107th Ave.
Miami, FL 33172
(305) 593-6033
▶ **CIRCLE 602**

▼ COMPACT OCXO OFFERS HIGH STABILITY



Temperature stability of ±6×10^{-9} from –20 to +70°C and aging of only ±7×10^{-10} per day is specified for the model 4840 oven-controlled crystal oscillator. The compact unit measures just 2 in.^{2} by 0.75 in. and covers the range of 7 to 15 MHz. Multiple options include sine or HCMOS outputs, 12- or 15-V supply, and electronic or mechanical frequency-control adjustment. Small quantities are available in 4 to 6 weeks, and large lots ship in 10 to 12 weeks. Call for pricing.

Oak Frequency Control Group
100 Watts St., P.O. Box B
Mt. Holly Springs, PA 17065
(717) 486-3411
▶ CIRCLE 603

▼ AXIAL-LEADED LEDs INCORPORATE RESISTOR

An integral resistor in series with the emitter chip is featured in the HLMP-6X00 and HLMP-6X20 Series of subminiature, T-3/4, axial-leaded LEDs. The 5-V devices' construction allows for operation in circuits with 5-V supply voltages without the use of an external current-limiting resistor. The plastic lamp packages have a square base design that's suitable for SMT applications. Typical luminous intensity is 5 mcd at 5 V for the -6X00 and 2 mcd at 5 V for the -6X20. Emitted colors include high-efficiency red, high-efficiency green, and yellow. Pricing starts at $0.46 for the -6X00 and $0.44 for the 6X20 in lots of 1000 and in bulk packaging. Lead times are 6 to 8 weeks for bulk orders and 8 to 10 weeks for tape and reel packaging.

Quality Technologies Corp.
610 N. Mary Ave.
Sunnyvale, CA 94086-2906
(408) 720-1440
▶ CIRCLE 604

▼ CAPACITORS SERVE HIGH-FREQUENCY TASKS

A line of high-density and high-frequency capacitors is intended for use in the input and output filter circuits of high-frequency dc-dc converters and switch-mode power supplies. The Capstick Type CS capacitors replace conventional types that are too high in impedance due to frequency-sensitive ac losses or exhibit excessive inductance because of size and shape. They offer low ESR and ESL and handle high ripple currents. Standard values range from 4.7 mF to 25 mF at 100 V dc with other ratings available. Call for pricing.

ITW Paktron
1205 McConville Rd.
Lynchburg, VA 24502
(804) 239-6941
▶ CIRCLE 605

PASSIVE-COMPONENT MANUFACTURERS

Electronic Concepts Inc.
526 Industrial Way West
Eatontown, NJ 07724
(908) 542-7880
(FL) (FP) (FY) (FT) (FF)
CIRCLE 832

Electronic Film Capacitors Inc.
41 Interstate Lane
Waterbury, CT 06705
(203) 755-5629
(FL) (FP) (FY) (FT)
CIRCLE 833

Electronic Precision Components
BG Electronics Div.
519 S. Fifth Ave.
Mt. Vernon, NY 10550-4407
(914) 664-5591
(AF) (IF) (RF) (PL) (PF)
CIRCLE 834

ELtech
181 Gibraltar Rd.
Horsham, PA 19044
(215) 441-0404
(UV)
CIRCLE 835

Ericsson Components Inc.
403 International Pkwy.
Suite 500
Richardson, TX 75081
(214) 669-9900
(EM)
CIRCLE 836

Fox Electronics
5570 Enterprise Pkwy.
Fort Myers, FL 33905
(813) 693-0099
(MC) (SC) (CL) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 837

Frequency Electronics Inc.
55 Charles Lindbergh Blvd.
Mitchel Field, NY 11553-3601
(516) 794-4500
(QC) (CL) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 838

Gowanda Electronics Corp.
1 Industrial Pl.
Gowanda, NY 14070
(716) 532-2234
(IF) (RF) (SU)
CIRCLE 839

Hewlett-Packard Co.
Components Div.
370 W. Trimble Rd.
San Jose, CA 95131-1008
(800) 357-7715
(FC) (ON) (EM) (IE)
(IS) (LL) (LI) (OI)
CIRCLE 840

Hirose Electric USA
2688 Westhills Ct.
Simi Valley, CA 93065
(805) 522-7958
(ON)
CIRCLE 841

Hokuriku USA Ltd.
200 N. Northwest Hwy.
Barrington, IL 60010
(708) 382-9411
(AU) (CF) (CE) (TF) (TH)
(MO) (CH) (ST) (TR) (RN)
CIRCLE 842

Honeywell Inc.
MICRO SWITCH
11 W. Spring St.
Freeport, IL 61032
(800) 537-6945
(EM) (IE) (IS) (LL) (LI)
(OI) (PD) (PT) (PR)
CIRCLE 843

IDEA Inc.
1300-B Pioneer St.
Brea, CA 92621
(310) 697-4332
(IS) (LL) (LI) (OI)
(PD) (PT) (PR)
CIRCLE 844

Il Stanley Co. Inc.
2660 Barranca Pkwy.
Irvine, CA 92714
(714) 222-0777
(IE) (IS) (LL) (LI) (OS)
(PH) (PD) (PR)
CIRCLE 845

ITW Paktron
1205 McConville Rd.
Lynchburg, VA 24502
(804) 239-6941
(FP) (FY) (CP) (CN)
CIRCLE 846

Illinois Capacitor Inc.
3757 W. Touhy Ave.
Lincolnwood, IL 60645
(708) 675-1760
(CD) (EA) (FL) (FP) (FY)
CIRCLE 847

Inductive Components & Crystal
10555 Dale Ave.
Stanton, CA 90680
(800) 899-3420
(AF) (IF) (RF) (SU) (MC)
(QC) (SC) (CL) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 848

International Mfg. Services Inc.
50 Schoolhouse Lane
Portsmouth, RI 02871-2418
(401) 683-9706
(CE) (TF) (TH) (HR) (CH)
CIRCLE 849

J.W. Miller
Div. of Bell Industries Inc.
306 E. Alondra
Gardena, CA 90248
(310) 515-1720
(IF) (RF) (SU)
CIRCLE 850

KCK America
Div. of Mitsubishi
4080 Winnetka Ave.
Rolling Meadows, IL 60008
(708) 577-0200
(CH) (CD) (CP) (SU) (PF)
CIRCLE 851

KEMET Electronics Corp.
P.O. Box 5928
Greenville, SC 29606
(803) 963-6589
(CM) (CP)
CIRCLE 852

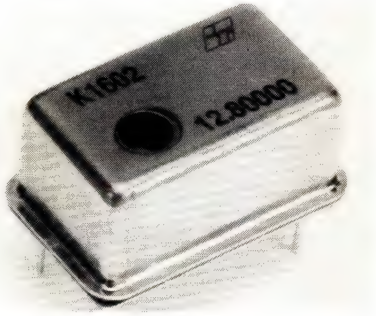
KOA Speer Electronics Inc.
P.O. Box 547, Bolivar Dr.
Bradford, PA 16701
(814) 362-5536
(CF) (MN) (TF) (TH) (HR)
(MO) (WW) (CH) (ST) (TR)
(RN) (CP) (SU)
CIRCLE 853

Kamaya Inc.
4000 Transportation Dr.
Fort Wayne, IN 46818
(219) 489-1533
(CF) (MN) (TF) (TH)
(MO) (CH) (RN)
CIRCLE 854

(see p. 130 for key)
(continued on p. 128)

▼ 2-PPM OSCILLATORS HAVE ADJUSTABLE OUTPUT

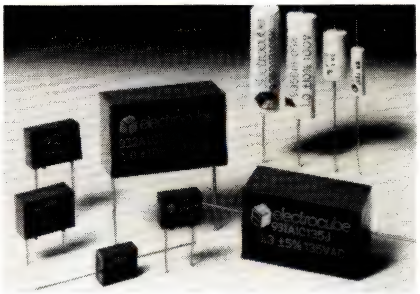
Stability of ±2 ppm over a temperature range of –40 to +85°C is featured by the K1602 Series of temperature-controlled crystal oscillators. Sinewave output is available for frequencies from 12 to 25 MHz and TTL output is offered from 3 to 25 MHz. Frequency is mechanically adjustable ±10 ppm/min by means of an internal trimmer. Call for pricing.



Champion Technologies Inc.
2553 N. Edgington St.
Franklin Park, IL 60131
(708) 451-1000
▶ **CIRCLE 606**

▼ POLY CAPACITORS EXTEND AC RATINGS

A wider range of ac voltages in a dry capacitor is featured by the Series 900 metallized polypropylene capacitors. Designed for pulse applications, the devices now are offered in 480 and 660 V ac, 50/60 Hz ratings. The new versions round out a line available in ratings of 67 V ac/100 V dc, 135 V ac/200 V dc, and 270 V ac/400 V dc. Capacitance values range from 0.0010 to 20 mF with tolerances to ±1%. Pricing is $0.59 in lots of 1000 (0.22 mF, 135 V ac/200 V dc, ±5%). Delivery is in 6 to 8 weeks.



Electrocube
1307 S. Myrtle Ave.
Monrovia, CA 91016
(818) 301-0122
▶ **CIRCLE 607**

PASSIVE-COMPONENT MANUFACTURERS

Lamp Technology Inc.
1645 Sycamore Ave.
Bohemia, NY 11716
(516) 567-1800
(LL)
CIRCLE 855

MF Electronics Corp.
10 Commerce Dr.
New Rochelle, NY 10801
(914) 576-6570
(MC) (QC) (CY) (VC)
(CK) (SO)
CIRCLE 856

MTI-Milliren Technologies Inc.
Two New Pasture Rd.
Newburyport, MA 01950
(508) 465-6064
(CY) (TC) (SO)
CIRCLE 857

Magnetic Technology Inc.
1237 Executive Dr. East
Richardson, TX 75081
(214) 480-8585
(AF) (IF) (RF) (SU)
CIRCLE 858

Marktech International Corp.
5 Hemlock St.
Latham, NY 12110
(518) 786-6591
(FC) (ON) (EM) (IE) (LL) (LI)
(OI) (PD) (PT) (PR)
CIRCLE 859

McCoy, Ovenaire, Spectrum, Croven
Oak Frequency Control
P.O. Box B, 100 Watts St.
Mount Holly Springs, PA 17065
(717) 486-3411
(QC) (SC) (CL) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 860

Micro Ohm Corp.
1088 Hamilton Rd.
Duarte, CA 91010
(818) 357-5377
(MN)
CIRCLE 861

Mini-Systems Inc.
Thin Film Div.
20 David Rd., P.O. Box 69
North Attleboro, MA 02761-0069
(508) 695-0203
(CR) (CE) (TF) (TH) (GL) (HR)
(CH) (RN) (CP) (CN)
CIRCLE 862

NEC Electronics Inc.
475 Ellis St., MS-MV4580
Mountain View, CA 94039
(800) 366-9782
(CM) (ED) (EM) (IE) (LL)
(LI) (OI) (PR)
CIRCLE 863

NTE Electronics Inc.
44 Farrand St.
Bloomfield, NJ 07003
(800) 631-1250
(MN) (MO) (WW) (CD) (EA)
(ED) (FP) (LL) (LI) (OI)
CIRCLE 864

North American Capacitor Co.
Mallory Div.
7545 Rockville Rd.
Indianapolis, IN 46214
(317) 273-0090
(WW) (CD) (CM) (EA) (ED)
(EW) (FL) (FP) (FY) (FT) (CP)
(VB)
CIRCLE 865

Ohmite Mfg. Co. Inc.
3601 W. Howard St.
Skokie, IL 60076
(708) 675-2600
(CC) (CF) (CR) (MN) (TF)
(GL) (HR) (WW) (ST) (RF)
CIRCLE 866

Optek Technology Inc.
1215 W. Crosby Rd.
Carrollton, TX 75006
(214) 323-2200
(EM) (IE) (IS) (LI) (OS)
(OI) (PD) (PT) (PR)
CIRCLE 867

Pico Electronics
453 N. MacQuesten Pkwy.
Mt. Vernon, NY 10522
(914) 699-5514
(SU)
CIRCLE 868

Piezo Crystal Co.
100 "K" St.
Carlisle, PA 17013
(717) 249-2151
(QC) (CY)
CIRCLE 869

Piezo Technology Inc.
2525 Shader Rd.
Orlando, FL 32804
(407) 298-2000
(QC) (SC) (CL) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 870

Prem Magnetics Inc.
3521 N. Chapel Hill Rd.
McHenry, IL 60050
(815) 385-2700
(AF) (RF) (SU)
CIRCLE 871

Quality Technologies Corp.
Custom/IR Products
2340 Trinity Mills, #330
Carrollton, TX 75006
(214) 418-2946
(IE) (IS) (LI) (OS) (PD) (PR)
CIRCLE 872

Quality Technologies Corp.
610 N. Mary Ave.
Sunnyvale, CA 94086
(408) 720-1440
(IE) (IS) (LL) (LI) (OS)
(OI) (PD) (PR)
CIRCLE 873

RCD Components Inc.
520 E. Industrial Park Dr.
Manchester, NH 03109
(603) 669-0054
(AU) (CF) (CR) (CE) (MN)
(TF) (TH) (GL) (HR) (MO)
(WW) (CH) (RN) (CN) (AF)
(IF) (RF) (SU) (PL)
CIRCLE 874

Raltron Electronics Corp.
2315 N.W. 107th Ave.
Miami, FL 33172
(305) 593-6033
(MC) (QC) (SC) (CL) (CY)
(TC) (VC) (CK) (SO)
CIRCLE 875

Renco Electronics Inc.
60 Jefryn Blvd. East
Deer Park, NY 11729
(516) 586-5566
(AF) (IF) (RF) (SU) (PF)
CIRCLE 876

Robert G. Allen Co. Inc.
7267 Coldwater Canyon
North Hollywood, CA 91605
(818) 765-8300
(CC) (CF) (CR) (CE) (TH)
(MO) (WW) (CH) (RN) (CD)
(CM) (EA) (EW) (FL) (FP)
(FY) (FT) (CP) (CN) (VB)
(IE) (IS) (LL) (LI)
CIRCLE 877

Rohm Corp.
3034 Owen Dr.
Antioch, TN 37103
(615) 641-2020
(CF) (MN) (MO) (CH) (RN)
(CM) (CP) (EM) (IE) (IS)
(LL) (LI) (PR)
CIRCLE 878

SI Tech
P.O. Box 609
Geneva, IL 60134
(708) 232-8640
(FC) (ON) (EM) (OI)
CIRCLE 879

Saronix
151 Laura Lane
Palo Alto, CA 94303
(415) 855-6887
(MC) (QC) (SC) (CL) (CY)
(TC) (VC) (CK) (SO)
CIRCLE 880

Shogyo International Corp.
287 Rt. 25A
Great Neck, NY 11021-4799
(516) 466-0911
(AF) (RF) (LL)
CIRCLE 881

Shokai Far East Ltd.
9 Elena Ct.
Peekskill, NY 10566
(914) 736-3500
(AU) (CF) (CE) (MN) (HR)
(MO) (WW) (CH) (ST) (MT)
(TR) (RN) (CD) (EA) (CP)
(CN) (VB) (AF) (IF) (RF) (SU)
(QC) (SC) (CL) (CY) (CK)
(SO) (IE) (IS) (LL) (LI) (PT)
CIRCLE 882

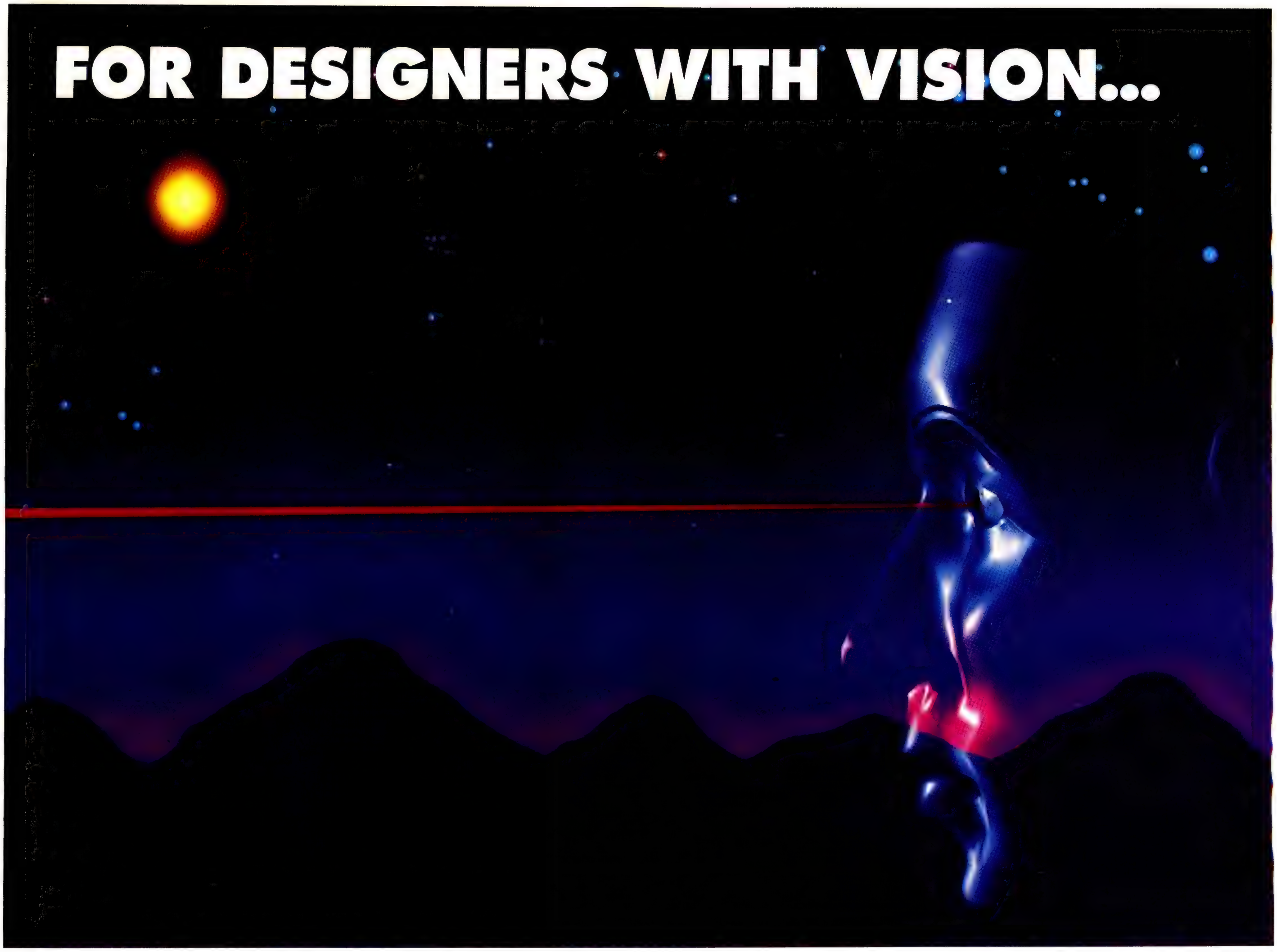
Siecor Corp.
P.O. Box 489
Hickory, NC 28603-0489
(704) 327-5000
(FC) (ON)
CIRCLE 883

Siemens Components Inc.
Special Products Div.
186 Wood Ave. South
Iselin, NJ 08830
(908) 906-4300
(CM) (EA) (ED) (EW) (FL)
(FP) (FY) (CP) (PF)
CIRCLE 884

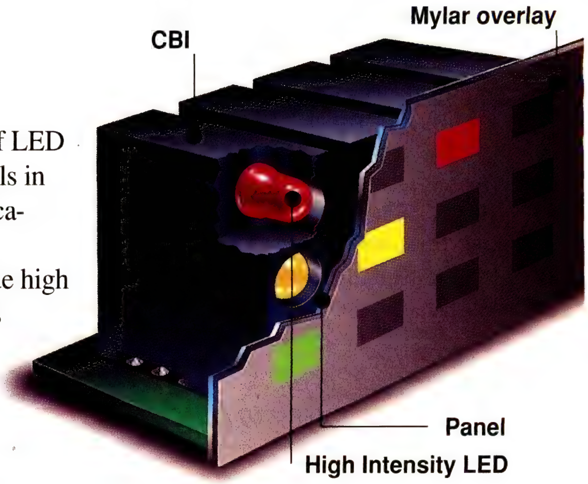
Siemens Fiber Optic Components
20 F Commerce Way
Totowa, NJ 07512
(201) 890-1606
(ON) (EM) (OS)
CIRCLE 885

Solitron Devices Inc.
Semiconductor Group
3301 Electronics Way
West Palm Beach, FL 33407
(407) 848-4311
(CR) (MN) (TH) (HR)
(CH) (TR) (RN)
CIRCLE 886

(see p. 130 for key)
(continued on p. 130)


FOR DESIGNERS WITH VISION...

New Dialight Backlights.



The advantages of backlighting — including ease of manufacture and enhanced panel appearance — are now a reality.

Introducing the Backlight CBI® Series, Dialight's advanced new family of LED circuit board indicators specially designed for backlighting legends and panels in data/telecommunications, industrial controls and a wide range of other applications.

Comprised of non-diffused LEDs, Dialight's backlighting products provide high intensity illumination. What's more, their unique right angle housing extends around the LED, minimizing light "bleed" to adjacent indicator apertures.

Select from 3mm singles, bi- and tri-levels, as well as 5mm singles and bi-levels.

Dialight. The industry leader in solutions for the application of LEDs.

Contact: Dialight Corp., Dept. C-BLI, 1913 Atlantic Ave., Manasquan, NJ 08736.

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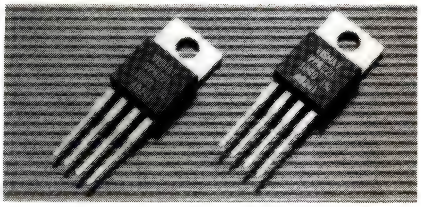
READER SERVICE 90

▼ POWER RESISTORS COME IN TO-220 PACKAGE

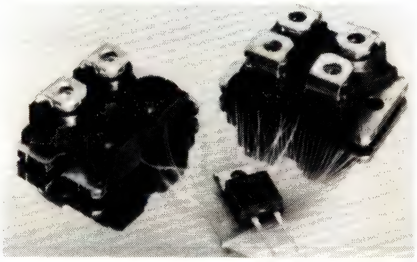
Two precision foil power resistors come packaged in TO-220 configurations. Model VPR 220 is a two-lead device while model VPR 221 has a four-lead Kelvin connection. Made from Vishay's Bulk Metal foil, both models offer low TCRs, high stability, tight tolerances, and fast response times. Power handling is rated at 8 W chassis mounted with a TCR of 5 ppm/°C. Tolerances are to ±0.01%. Call for pricing.



Vishay Resistors
63 Lincoln Hwy.
Malvern, PA 19355
(215) 644-1300
▶CIRCLE 608

▼ POWER RESISTOR FOR PULSE LOADS

The Type HXP power resistor is offered in tolerances of ±1, ±2, ±5, and ±10% with temperature coefficients of ±25, ±50, and ±100 ppm/°C. The maximum power rating for the non-inductive devices at 25°C is 100 W. The units are supplied with two-terminal or four-terminal connections. Applications include high-frequency circuits or pulse loads. Call for pricing and delivery.



EBG Inc.
3705 Trindle Rd.
Camp Hill, PA 17011-4335
(717) 737-9877
▶CIRCLE 609

▼ CHIP CAPS HANDLE HIGH INRUSH CURRENTS

Designed primarily for output filtering in switch-mode supplies and dc-dc converters, the T495 Series of low-ESR tantalum chip capacitors is also a good choice for battery-to-ground input filtering. Values from 4.7 to 150 µF are offered with voltage ratings from 6 to 50 V dc. Features include high ripple-current capability, reduced dissipation factor and dc-leakage levels, and an improved ability to handle high inrush currents. Call for pricing and delivery.

KEMET Electronics Corp.
P.O. Box 5928
Greenville, SC 29606
(803) 967-6875
▶CIRCLE 610

PASSIVE-COMPONENT MANUFACTURERS

Spectrol Electronics Corp.
4051 Greystone Dr.
Ontario, CA 91761
(909) 923-3313
(ST) (MY) (TR)
CIRCLE 887

Sprague-Goodman Electronics
134 Fulton Ave.
Garden City Park, NY 11040
(516) 746-1385
(AI) (CM) (FL) (FY) (GC)
(MI) (VB) (SU)
CIRCLE 888

Standard Crystal Corp.
9940 E. Baldwin Pl.
El Monte, CA 91731
(818) 443-2121
(MC) (QC) (SC) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 889

State of the Art Inc.
2470 Fox Hill Rd.
State College, PA 16803-1797
(814) 355-8004
(TF) (TH) (HR) (SU)
CIRCLE 890

Tele Quartz Group GmbH
Landstrasse, D-74924
Neckarbischofsheim 2
Germany
(49) 07268/8010
(MC) (QC) (SC) (CL) (CY)
(TC) (VC) (CK) (SO)
CIRCLE 891

Thermometrics Inc.
Bowthorpe
808 U.S. Hwy. 1
Edison, NJ 08817
(908) 287-2870
(MO) (IS)
CIRCLE 892

Toko America Inc.
1250 Feehanville Dr.
Mount Prospect, IL 60056
(708) 297-0070
(AF) (IF) (RF) (SU) (PL) (PF)
CIRCLE 893

Toshiba Marcon Electronics America Corp.
998 Forest Edge Dr.
Vernon Hills, IL 60061
(708) 913-9980
(MO) (CM) (EA) (ED)
(EW) (FP) (FY) (CP)
CIRCLE 894

US Conec Ltd.
P.O. Box 2306
Hickory, NC 28603-2306
(704) 323-8883
(ON)
CIRCLE 895

Valor Electronics Inc.
9715 Business Park Ave.
San Diego, CA 92131
(619) 537-2500
(RF) (SU) (PL) (PF)
CIRCLE 896

Valpey-Fisher Corp.
75 South St.
Hopkinton, MA 01748
(508) 435-6831
(MC) (QC) (SC) (CY) (TC)
(VC) (CK) (SO)
CIRCLE 897

Vectron Laboratories Inc.
166 Glover Ave.
Norwalk, CT 06850
(203) 853-4433
(CY) (TC) (VC) (CK) (SO)
CIRCLE 898

Vishay Electronic Components U.S.
1122 213rd St.
Columbus, NE 68601-3647
(402) 563-6350
(MN) (TF) (TH) (HR) (MO)
(WW) (CH) (ST) (MT) (TR)
(RN) (ED) (EW) (FL) (FP) (FY)
(CP) (AF) (IF) (RF) (SU) (PF)
(CK) (SO)
CIRCLE 899

Vishay Resistors Systems
63 Lincoln Hwy.
Malvern, PA 19355
(215) 251-5267
(AU) (TF) (TH) (GL) (HR)
(CH) (TR) (RN)
CIRCLE 900

KEY

Resistors

(AU)	Audio
(CC)	Carbon composition
(CF)	Carbon film
(CR)	Ceramic
(CE)	Cermet
(MN)	Metal/non-metal film
(TF)	Thick film
(TH)	Thin film
(GL)	Glass
(HR)	High resistance
(MO)	Metal oxide
(WW)	Wire-wound
(CH)	Chip
(CO)	Conductive plastic
(ST)	Single-turn pot
(MT)	Multi-turn pot
(TR)	Trimmers
(RN)	Resistor networks

Capacitors

(AI)	Air
(CD)	Ceramic/disk
(CM)	Ceramic/multilayer
(EA)	Electrolytic/aluminum
(ED)	Electrolytic/tantalum dry slug
(EW)	Electrolytic/tantalum wet
(FL)	Film/polycarbonate
(FP)	Film/polyester
(FY)	Film/polypropylene
(FT)	Film/polystyrene
(FF)	Film/polysulfone
(CG)	Glass
(MI)	Mica
(TE)	Teflon
(VA)	Vacuum
(CP)	Chip
(CN)	Capacitor networks
(VB)	Variable capacitors

Inductors, Coils, and Chokes

(AF)	Audio frequency
(IF)	Intermediate frequency
(RF)	Radio frequency
(SU)	Surface-mounted
(PL)	Passive delay lines
(PF)	Passive filters

Crystals and Oscillators

(MC)	Microprocessor crystals
(QC)	Quartz crystals
(SC)	Surface-mounted crystals
(CL)	Crystal filters
(CY)	Crystal oscillators
(TC)	Temperature-controlled oscillators
(VC)	Voltage-controlled oscillators
(CK)	Clock oscillators
(SO)	Surface-mounted oscillators

Optoelectronics

(EL)	Electroluminescents
(FC)	Fiber-optic cables
(ON)	Fiber-optic connectors
(EM)	Fiber-optic emitters/detectors
(IE)	Infrared emitters
(IS)	Infrared sensors
(LL)	LEDs, light-emitting
(LI)	LEDs, IR-emitting
(OS)	Optical switches
(OI)	Optocouplers/isolators
(PH)	Photocells
(PC)	Photoconductive cells
(PD)	Photodarlingtons
(PT)	Photodiodes and arrays
(PR)	Phototransistors
(UV)	UV sensors

Congratulations, Apple, on a day we've both looked forward to seeing.

IBM Microelectronics
Total Technology Solutions

On March 14th Apple launched Power Macintosh™ systems, a family of personal computers using our revolutionary, RISC-based PowerPC™ microprocessors. As a member of the PowerPC alliance with Apple and Motorola, we're proud to see such tangible proof that our vision has become a reality. Yet while IBM is delighted to celebrate today, we're still determined to anticipate tomorrow. With products, applications and support designed to make PowerPC microprocessors, and the systems they run, the future of computing. It's a challenge IBM Microelectronics™ Division and Apple welcome. In fact, we look forward to it.

IBM®

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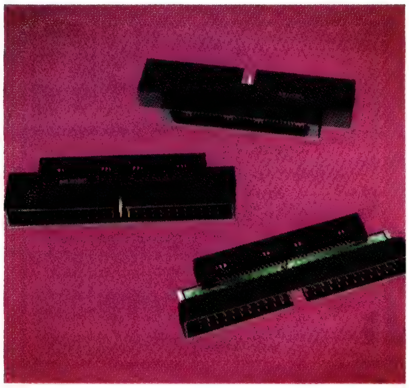
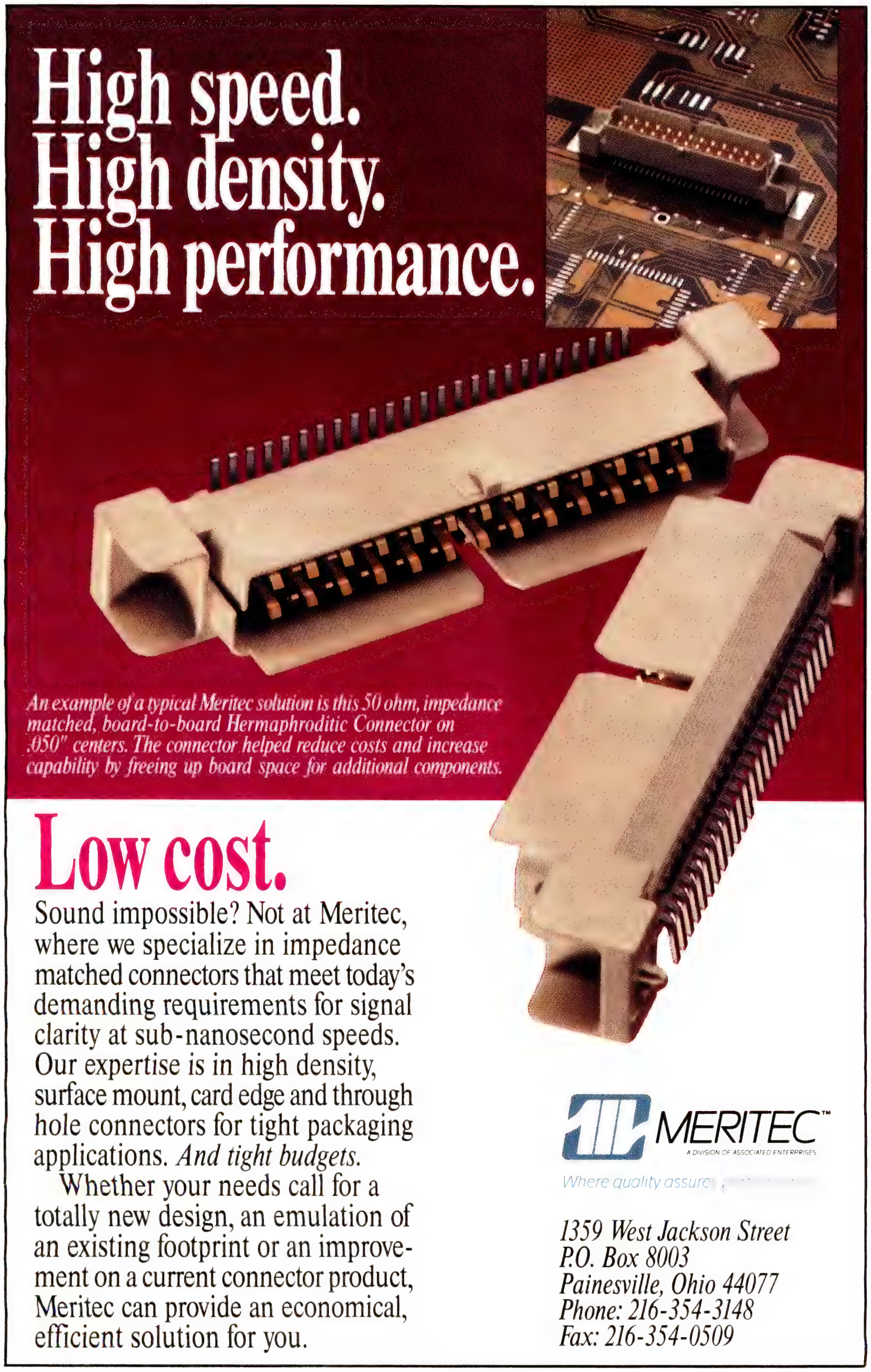
READER SERVICE 225

8-Bit to 16-Bit Male-to-Male SCSI Interface Adapters



Meritec's 50 position male to 68 position male SCSI Interface Adapters allow reliable interfacing of 8-bit to 16-bit and 16-bit to 8-bit devices. The adapters eliminate the need for multiple cable assembly configurations which would otherwise be needed to interface the two types of devices. The adapter mates with 50 position .100 x .100 grid SCSI-1 receptacles and 68 position .050 x .100 grid SCSI-3 receptacles. Short overall length between the mating faces of the adapter allows dense packaging. Customer-specific pinouts, filtering and terminations are available.

READER SERVICE 104



High speed.
High density.
High performance.

An example of a typical Meritec solution is this 50 ohm, impedance matched, board-to-board Hermaphroditic Connector on .050" centers. The connector helped reduce costs and increase capability by freeing up board space for additional components.

Low cost.

Sound impossible? Not at Meritec, where we specialize in impedance matched connectors that meet today's demanding requirements for signal clarity at sub-nanosecond speeds. Our expertise is in high density, surface mount, card edge and through hole connectors for tight packaging applications. *And tight budgets.*

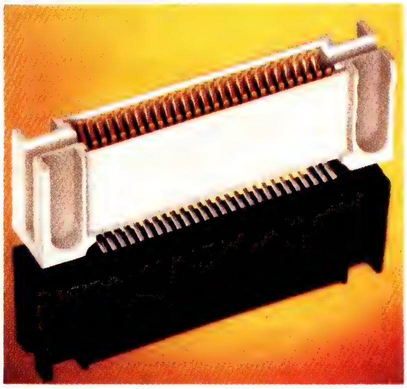
Whether your needs call for a totally new design, an emulation of an existing footprint or an improvement on a current connector product, Meritec can provide an economical, efficient solution for you.

MERITEC™
A DIVISION OF ASSOCIATED ENTERPRISES
Where quality assure

1359 West Jackson Street
P.O. Box 8003
Painesville, Ohio 44077
Phone: 216-354-3148
Fax: 216-354-0509

READER SERVICE 107

50 ohm Impedance Matched Card Edge Connectors



Meritec's high density CP50™ Card Edge Connectors are designed with .050" centers to minimize board space requirements. The 50 ohm, impedance matched connectors are ideal for high density board-to-board applications. The connectors are designed to meet IR or vapor phase reflow requirements. Through hole and SMT contact tail configurations are available. Precision, high strength molded terminations provide high reliability in critical applications.

READER SERVICE 105

High Density Hermaphroditic Connectors

Meritec's 50 ohm, impedance matched CP50™ Hermaphroditic Connectors feature .050" centers, with board spacing as close as .394" (10 mm), making them ideal for dense package applications. Two, three and four row designs are possible, in straight or right angle configurations, with through hole or SMT contact tails. Precision, high strength molded terminations provide high reliability in critical applications. The connectors are designed to meet IR or vapor phase reflow requirements.

READER SERVICE 106

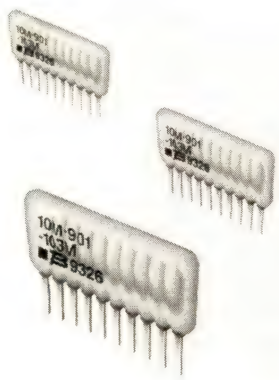
▼ HIGH-BRIGHTNESS LEDs NOW COME IN CHIP FORM

Tiny chip LEDs with brightness levels to 40 mcd are available from ROHM. The SML 010 Series LEDs have no leads protruding from the package exterior. Instead, these devices feature electrodes built into the chip material in the fashion of SMT components. Luminous intensity for the red LEDs ranges from 40 mcd for the ultra-bright SML 010JT to 16 mcd for the high-brightness SML 010LT, both at 20 mA. Peak wavelength for both is 660 nm and viewing angle is 100°. Pricing is $0.18 for the -LT and $0.28 for the -JT, both in lots of 10,000. Delivery is in 6 to 8 weeks.

ROHM Corp.
Electronics Div.
3034 Owen Dr.
Antioch, TN 37013
(615) 641-2020, ext. 121.
▶ CIRCLE 611

▼ CAPACITOR NETWORKS HAVE VARIOUS USES

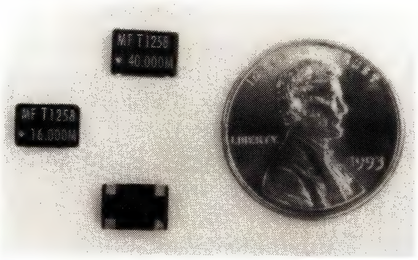
A series of low-cost capacitor networks is available for use in bypassing, filtering, coupling, and termination in IC applications. The 900 Series networks comes in standard bussed or isolated circuit configurations and in medium or high profiles. Packaging is in conformally coated SIPs with from four to 14 pins. The devices offer superior noise suppression, high reliability, and lower component counts on pc boards. Prices begin at $1.43 for the 4610M-901 (bussed) network and $0.86 for the 4610M-902 (isolated) type, both in lots of 500.



Bourns Inc.
Integrated Technologies Div.
1400 North 1000 West
Logan, UT 84321
(801) 750-7200
▶ CIRCLE 612

▼ TINY OSCILLATOR WITHSTANDS EXTREMES

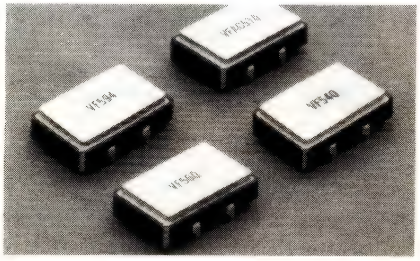
Like the rest of the T Series of SMT crystal clock oscillators, the model T1258 micromini oscillator drives full-sized 50-pF (HCMOS) or 10 TTL loads. But in addition, the T1258 oscillator can handle these loads over an extended industrial temperature range of –40 to +85°C. The device measures 5 by 7 mm with a height of 2.3 mm. Frequency stability is ±0.01% over a frequency range of 1.8 to 50 MHz. Ruggedness and reliability are enhanced by a truly hermetic glass-ceramic seal. Pricing is $6.50 in lots of 1000. Delivery is in 4 to 6 weeks.



MF Electronics Corp.
10 Commerce Dr.
New Rochelle, NY 10801
(914) 576-6570
▶ CIRCLE 613

▼ TRUE SMT OSCILLATOR WON'T WASTE PCB SPACE

A true miniature SMT package for hybrid oscillators measures just 0.55 in. long, 0.35 in. wide, and 0.185 in. tall. The ceramic package houses oscillators in the frequency range of 2 to 300 MHz with TTL, HCMOS, ACMOS, and ECL logic options. All types are capable of operating in a wide temperature range and with high frequency stability. The package is hermetically seam welded with a nickel-plated Kovar lid and has J-lead terminations that match the 0.200-by-0.300-in. footprint of common plastic oscillator packages. Pricing ranges from $10 to $33 depending on specifications and delivery is in 8 weeks.



Valpey-Fisher Corp.
75 South St.
Hopkinton, MA 01748
(508) 435-6831
▶ CIRCLE 614

▼ HEATED OSCILLATOR MAINTAINS STABILITY

By mounting a heating element directly on an SC-cut crystal blank, a crystal oscillator is created that bridges the gap between temperature-controlled and oven-controlled crystal oscillators. Piezo Crystal's directly-heated crystal oscillator (DHXO) is designed for engineers whose system needs better phase noise and vibrational sensitivity than a TCXO can offer, but still needs low current consumption. Also, some systems need the phase noise and vibrational sensitivity of an OCXO, but not their stability or input current. Units are offered in the frequency range of 7 to 15 MHz with operation from –20 to +70°C. Frequency stability over that range is $\pm2\times10^{-7}$. From zero to +60°C, stability is $\pm1\times10^{-7}$. Warm-up time to full-range stability is in less than 3 minutes. Call for pricing and delivery.

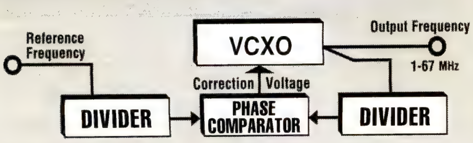
Piezo Crystal Co.
100 K St.
P.O. Box 619
Carlisle, PA 17013
(717) 249-2151
▶ CIRCLE 615

MF ELECTRONICS CORP.

VCXO's and PHASE-LOCKED-LOOP-VCXO

VCXO's Series M2000
1MHz to 67 Mhz

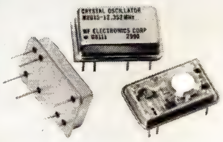
These VCXO's are used to replace a distorted incoming reference signal (e.g. 1.544 MHz, T1), with a stable crystal-controlled signal of the same or any multiple frequency, from 1 to 67 MHz.



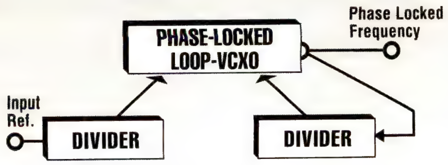
With MF VCXO's, since the specification is computer-tested over the full operating temperatures, you can be assured that the specified frequency- deviation is what you get for capture range.

	Control Voltage	Deviation
M2001	0.3 to 10V	±175 ppm
M2002	0.3 to 4V	± 75 ppm
M2003	0.3 to 10V	±175-300 ppm
M2004	0.3 to 4V	±125 ppm
M2005	1.0 to 4V	± 75-300 ppm
M2006	0 to 5V	±150 ppm
M2007	0.5 to 4.5V	±125-250 ppm

PHASE-LOCKED LOOP-VCXO'S
Series M2010, M2015

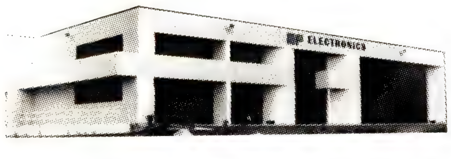


This is the complete loop, including the phase-comparator and the VCXO, in just one package. Add the dividers to match the frequencies. Oscillators from 10 to 30MHz.



	Frequency Range
M2010	±125 ppm
M2015	±150 ppm

READER SERVICE 200



Headquarters and manufacturing plant: 36,000 sq. feet

MF ELECTRONICS CORP.
10 Commerce Drive
New Rochelle, NY 10801
914-576-6570 Fax: 914-576-6204

PASSIVE COMPONENTS

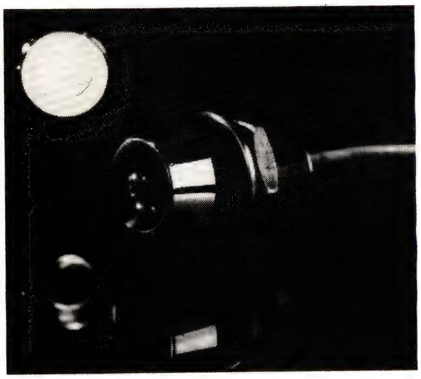
▼ TANTALUM CHIP CAPS SUIT PORTABLE TASKS

The TPS line of tantalum chip capacitors features low ESR values and high efficiency for use in power supplies for notebook computers, PDAs, PCMCIA drives, dc-dc converters, and cellular phones. Capacitance values range from 4.7 to 330 μF in EIA C and D case sizes. The parts are capable of higher ripple currents, lower ripple voltages, and less power and heat dissipation than competing devices. Call for pricing and delivery.

AVX Corp.
801 17th Ave. South
Myrtle Beach, SC 29577
(803) 946-0690
▶ CIRCLE 616

▼ ULTRA-BRIGHT LEDs OUTSHINE THE SUN

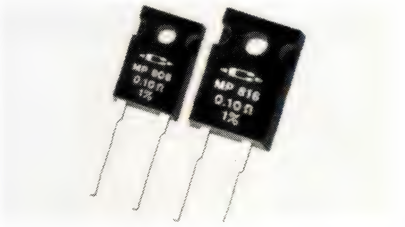
A packaged AlInGaP LED features a luminous-intensity rating of 3000 mcd, which makes it suitable for high-brightness indication and outdoor sunlight applications. The DDP 200-A3K LED is available in a variety of lamp bases, panel-mounted, and pc-board configurations. It a peak wavelength of 594 nm, the high-intensity amber LED is offered in a water-tight panel mount (PMR200-A3K) with a voltage range of 5 V dc to 220 V ac. Life span is rated at 100,000 hours in applications requiring ultra-bright illumination of switches, lenses, and legends. Pric ing is $2.66 per thousand.



Data Display Products
445 S. Douglas St.
El Segundo, CA 90245-4630
(310) 640-0442
▶ CIRCLE 617

▼ TO-126 POWER RESISTORS HANDLE 8 W AT 25°C

The terminal attachment and resistance-element geometry used in Cac dock's Model MP808 power resisto combine to provide outstanding nor inductive performance. The TO-126 style device's body is completely sur rounded by a molding compoun with high thermal conductivity to fa cilitate power handling of 8 W at case temperature of 25°C derated t zero at 150°C. Resistances are o fered from 0.1 Ω to 10 kΩ. Standar tolerance is ±1% with others avai able. Pricing for a 50-Ω, 1% device i lots of 10,000 is $0.86.



Caddock Electronics Inc.
Applications Engineering
17271 N. Umpqua Hwy.
Roseburg, OR 97470
(503) 496-0700
▶ CIRCLE 618

▼ RESISTOR NETWORK OFFERS NARROW WIDTH

Surface-mount technology in small-outline (0.015-in width) pacl age is offered by the Model 4900P r sistor network. The device is avai able in pin counts of 8, 14, and 16 either isolated or bussed circuits. A vantages include drop-in replac ment capability, an integration lev that's higher than that of a mediur width package, a molded epoxy boc that allows for excellent therma shock performance, and electropla ed copper leads for high solderab ity. Pricing begins at $0.20.

Bourns Inc.
Integrated Technologies Div.
1400 N. 1000 West
Logan, UT 84321
(801) 750-7200
▶ CIRCLE 619

ADVANCED PORTABLE POWER

HIGHEST VOLUMETRIC DENSITY REGULAR NICd (1.2V Slim)

Maximum volumetric energy to deliver 50% higher discharge capacity than standard NiCd batteries. Features: superior gas absorption; 1.5 Hr. quick charge; superior shock and vibration resistance; low profile.

LOW PROFILE, HIGH VOLTAGE, RECHARGEABLE LITHIUM MANGANESE DIOXIDE (coin cell)

Features: High discharge voltage of 3V...twice conventional rechargeable NiCd button cells; superior storage characteristics; excellent discharge characteristics; 3000 cycles at charge/discharge condition of 1mAh per cycle.
Great choice for memory back-up or power interruption applications.

HIGH DENSITY NICKEL METAL HYDRIDE (Twicells)

Sanyo's proprietary Hydrogen absorbing electrode manufacturing process and built-in resealable vent, lead the development of high capacity, high performance rechargeable NiMH batteries.

ADVANCED, COST-EFFECTIVE, HIGH-PERFORMANCE Ni-Cd (Extra)

Incorporates high-density electrode plates in a NEW design concept for 40% greater capacity than conventional batteries.
Sanyo's -ΔV and Peak Voltage Sensor (PVS) charging method yields 1 Hr. charge time.

SANYO

SANYO Energy
(U.S.A.) Corporation
2001 Sanyo Avenue
San Diego, CA 92173

In Florida: 904/376-[illegible]711
In Illinois: 708/285-0333
In New Jersey: 201/64[illegible]-2333
In Georgia: 404/279-737[illegible]
In Dallas: 214/480-8345
In San Diego: 619/661-6620

READER SERVICE 204

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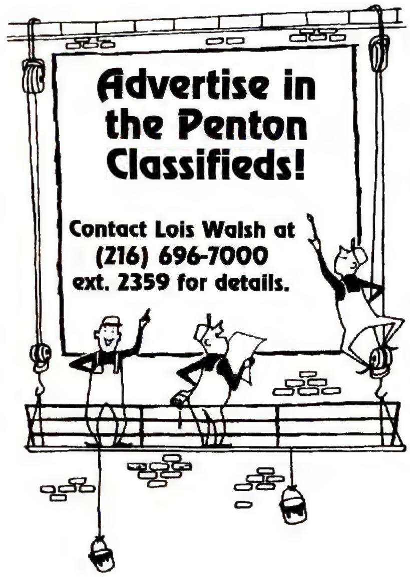
EMPLOYMENT OPPORTUNITIES

Electronics Design Engineer: Will use principles of adaptive and digital signal processing to modify and develop an electro graphic neurofeedback system. Will develop and improve software interface and insure proper integration with hardware design including development of small signal amplifiers and filters. Will use C and C++ to modify software. Requires Master's or completion of coursework for Master's degree in Electrical Engineering. Education to include completion of one course in which small signal amplifiers and filters were studied; one course in Electro Biomedicine; a laboratory course in Electrophysiology; one course in Medical Instruments; one course in Adaptive Signal Processing; and, one course in Random Signal Processing. Hours: 8:30 a.m.-5:00 p.m. 40 hours per week at $39,500 per year salary. Must have proof of legal authority to work permanently in the U.S. Please send two copies of resume to: Illinois Department of Employment Security, 401 S. State St. - 3 South, Chicago, IL 60605, ATTN: Pete Kula, Ref. #V-IL 11119-K, An Employer Paid Ad.

SOFTWARE

"XFMR 4.0"
DESIGN SOFTWARE 50Hz-500kHz. 3 Times faster than the best calculator. 6 Topologies 10 core types. Output: 56 computed values- AC resistance and Temp. rise. Order yours today! $59.50 IBM 5 1/4. Ph 407-277-6424. **NATIONWIDE ENGINEERING-ORLANDO, FL.**

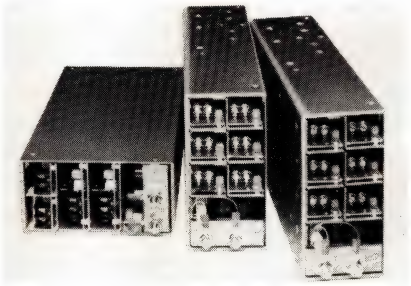


Advertise in the Penton Classifieds!
Contact Lois Walsh at (216) 696-7000 ext. 2359 for details.

POWER SOURCES

▼ SWITCHING SUPPLIES POWER BUS SYSTEMS

Single- and multiple-output switching power supplies are available for powering bus systems such as VME, VXI, and Futurebus. These units are based on the company's modular, high-density, open-frame Moduflex switchers. Four single-output VM Series units offer maximum power ratings from 750 to 864 W and power densities up to 10 W/in.^{3}. Four VX Series units offer seven outputs, VXIbus power-supply voltages, and maximum power of 500, 750, 1000, and 1500 W. Pricing starts at $479 for a quad-output, 400-W unit.



Deltron Inc.
290 Wissahickon Ave.
P.O. Box 1369
North Wales, PA 19454
(215) 699-9261
▶ **CIRCLE 620**

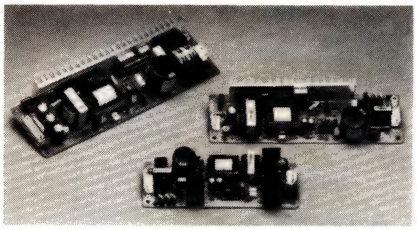
▼ HIGH EFFICIENCY MARKS 25-W CONVERTERS

A family of single-, dual-, and triple-output 25-W dc-dc converters is distinguished by a wide input range and high efficiency. The 2500 Series converters comprise 27 models that operate over 2:1 input ranges of 9 to 18 V dc, 18 to 36 V dc, or 36 to 72 V dc. Tightly regulated output combinations come from among 5, 6, 12, 15, ±5, ±12, and ±15 V dc. Features include 500-V dc input-to-output isolation, efficiencies as high as 85%, continuous short-circuit protection, and low output ripple and noise. Output-voltage accuracy is ±1% and line/load regulation is ±0.5%. Pricing starts at $90.30 with delivery from stock to 4 weeks.

Conversion Devices Inc.
15 Jonathan Dr.
Brockton, MA 02401
(508) 559-0880
▶ **CIRCLE 621**

▼ ECONOMICAL SWITCHERS ARE BUILT FOR EASE

A cost-effective layout that's structured for easy installation is featured in the LS/LU Series of single-output switching power supplies. Despite their relatively low price, the units offer high density, high isolation, and low profile. The LS Series offers worldwide 85-to-132 V ac input, while the LU Series accepts from 170 to 264 V ac. Versions providing 30, 50, and 100 W are offered with output voltages of 5, 12, 15, 24, and 48 V. Call for pricing and delivery.



Toko America Inc.
1250 Feehanville Dr.
Mount Prospect, IL 60056
(708) 297-0070
▶ **CIRCLE 622**

▼ SWITCHERS' LOW NOISE APPROACHES LINEARS

A low-output-noise version of the Easymod family of 3-by-5-in. switchers offers noise levels that, in many cases, are equivalent to existing linear products. The units come in 40- to 120-W, single- and multiple-output styles and feature universal ac inputs. Output noise is less than 10 mV pk-pk (5 mV typical). Easymod supplies can be modified to specific user requirements in quantities as low as 100 units per year. Typical turnaround for prototype/approval samples is from 4 to 6 weeks with production lead time from 6 to 8 weeks.

Power Solutions Inc.
4699 N. Federal Hwy.
Pompano Beach, FL 33064
(305) 943-4110
▶ **CIRCLE 623**

We're making a name for ourselves.

Energizer Power Systems was formed to provide OEMs a single source for primary and rechargeable power. With one of the industry's broadest product lines and a solutions approach to new portable product design, we're committed to meeting the power needs of the OEM community.

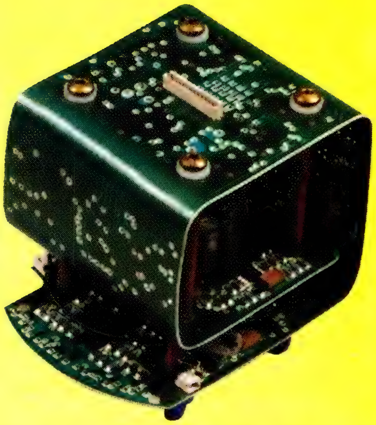
Featuring leading edge products like primary lithium and rechargeable nickel hydride, Energizer Power Systems offers superior design assistance, unsurpassed aftermarket presence and comprehensive power systems for today's competitive OEM marketplace.

Your partner in power.

For more information, call 1-800-67-POWER.

Energizer®
POWER SYSTEMS
A Division of Eveready Battery Company, Inc.

READER SERVICE 190



SPARTON ELECTRONICS

WILL BEND OVER BACKWARDS
for you, and that's what you expect from a world leader in full service custom manufacturing.
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with the most innovative, flexible and reliable practices available:
CAD
CONCURRENT ENGINEERING
DESIGN FOR MANUFACTURING
STATISTICAL PROCESS CONTROL
COMPLETE ELECTRONIC MANUFACTURING CAPABILITY
JUST-IN-TIME DELIVERY
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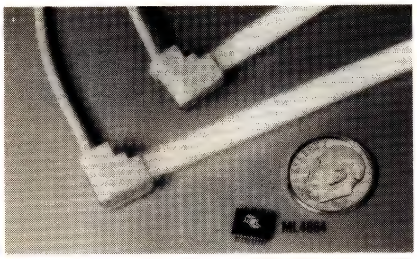
READER SERVICE 199

▼ BACKLIGHT IC POWERS NOTEBOOK, PDA LIGHTING

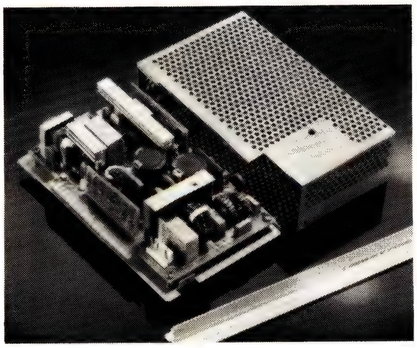
A BiCMOS chip produces the high voltages needed to drive miniature cold-cathode fluorescent lamps used to backlight LCDs in notebook computers and PDAs. The ML4864 chip also provides the contrast voltage required for LCDs. The device's input and output voltages can be set to almost any level with standard external components. Its fluorescent-lamp output is alternating current. A power-down mode independently shuts off the chip's high-voltage lamp-driver circuits while maintaining the LCD's contrast voltage. This feature extends battery life in bright ambient-light conditions by allowing a computer to display data while its backlight is turned off. Pricing for a 20-pin SSOP is $2.95 in lots of 1000.



Micro Linear Corp.
2092 Concourse Dr.
San Jose, CA 95131
(408) 433-5200
▶ **CIRCLE 624**

▼ SCALABLE SUPPLY IS ALSO PARALLELABLE

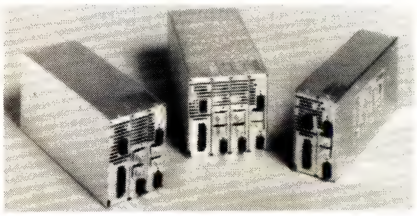
A scalable, parallelable 125-W ac-dc switching power supply delivers a 56-V output while taking 50% less space than conventional models. The SPA-125 supply is designed for critical systems that must run even when line power fails. Features of the fully enclosed supply include N+1 redundancy, Class B EMI filtering, built-in thermal protection, remote on-off, power-fail signal, and compatibility with the company's 20-to-180-W dc-dc converters.



MicroENERGY Inc.
745 W. State Road 434
Longwood, FL 32750-4909
(407) 831-2000
▶ **CIRCLE 625**

▼ HIGH-WATTAGE SUPPLIES OFFER HIGH EFFICIENCIES

A series of high-wattage modular power supplies features zero-voltage switching at 500 kHz that yields efficiencies of 80 to 90% with a front end that actively corrects power factor to 0.99. Models are available with outputs from 500 to 1750 W and with off-the-shelf modules that permit configurations of up to nine fully isolated outputs with a range of 2 to 48 V dc. All modules provide direct paralleling, current sharing, and N+1 redundancy. Pricing with power-factor correction and three outputs is $670 in lots of 100.



Omega Power Systems Inc.
8968 Fullbright Ave.
Chatsworth, CA 91311
(818) 727-2216
▶ **CIRCLE 626**

▼ LAB POWER SUPPLIES OFFER HIGH STABILITY

Available in single-, dual-, and triple-output models with ratings from zero to 30 V dc at 2.5 A per unit module, the AX320 Series of laboratory power supplies features output-voltage stability of under 10 mV for mains variation from 110 to 120 V dc, and under 20 mV for load variations from zero to 2.5 A. Adjustments to maximum current is between zero and 2.5 A. Low residual noise is rated at under 1 mV effective rms, maximum voltage to ground at 50 V, and common-mode voltage at 50 V peak. Resolution is 0.1 V and 10 mA with accuracy at 0.5%. Pricing starts at $395 for the single-output AX321.

ITT Instruments
1500 E. 9th St.
Pomona, CA 91766-3835
(909) 469-2900
▶ **CIRCLE 627**

Interpoint's MIL-STD-883 dc-dc converters:

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HI-REL DC-DC Converters for Every Power Level

Series	V in	V out	Outputs	Power
MSA	16 to 40	5,12,15	1 or 2	5 W
MHF+	16 to 40	5,12,15	1 or 2	15 W
MTR	16 to 40	5,12,15	1, 2, or 3	30 W
MFL	16 to 40 80 to 160 160 to 400	5,12,15,28	1 or 2	65 W*
MFLHP	19 to 40	5,12,15	1 or 2	100 W*

** Multiple units current share*

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Interpoint is recognized for innovation. Our 20-year history of breakthroughs includes the first 70 W/in^3 board-mountable dc-dc converters.

Interpoint is recognized for reliability. Our power supplies have logged more than 1,000,000 field hours per failure.

Our new, fully compliant MSA Series offers 5 watts of power in a case just 0.27" high. The MSA also meets MIL-STD-704A input voltages (up to 80V surges) with 5, 12, and 15 Vdc outputs.

For your **FREE HI-REL DESIGN FIELD KIT,** with Guides to selecting and using dc-dc converters in HI-REL systems, call:

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- Time constant of 15 seconds
- Operating range from -- 50° to +150°C
- Temperature accuracy of ±1°C @ 25°C
- Just over one inch long overall

R₀ @ 25°C	Temp. Coef. %/°C @ 25°C	Material
2K	–3.83	MS 73
5K	–4.43	MS 95
10K	–4.40	MS 97
30K	–4.32	MS 96
50K	–4.84	MS120
100K	–4.78	MS122

Other resistance values available.

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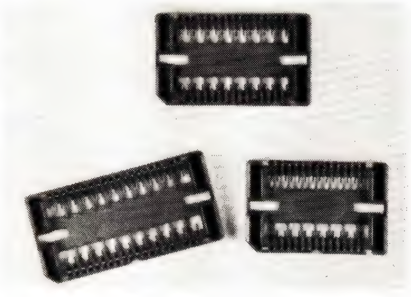
READER SERVICE 165

▼ LOW-PROFILE SOCKETS SEAT J-LEAD DEVICES

A series of small-outline, J-leaded chip carrier sockets is designed to accept 0.050-in. devices such as DRAMs and VRAMs for surface-mount termination to pc boards. The 665-SOJ Series sockets feature a very low profile of 0.177 in. above the board. Their high-temperature insulators are suited for vapor-phase or IR soldering. Sockets are offered in 28, 32, and 40 pin positions on 0.421-in. centers and 24, 26, 28, and 32 pin positions on 0.317-in centers. Typical unit pricing is $1.54 in small lots. Delivery is from stock to 4 weeks.



Andon Electronics Corp.
4 Court Dr.
Lincoln, RI 02865
(401) 333-0388
▶ CIRCLE 628

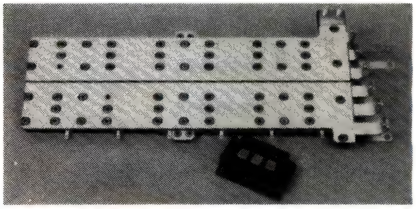
▼ PHONE PLUGS OFFER NICKEL-PLATED CONTACTS

Nickel plating is now offered, at no additional cost, on two popular series of phone plugs. The corrosion-resistant, nickel-plated plug fingers eliminate the need for frequent cleaning and reduce signal noise. The 482 and 483 (shown) three-conductor, 1/4-in. phone plugs can be ordered with standard brass tip rod or nickel-plated brass by adding the suffix N. The TT253 and TT254 bantam-type three-conductor TT (tiny telephone) plugs can also be ordered with nickel plating. Unit pricing is in the $10 range for small quantities of the 482N and 483N and in the $7 range for similar lots of the TT253N and TT254N. Delivery is in 6 to 8 weeks.

Switchcraft Inc.
5555 N. Elston Ave.
Chicago, IL 60630
(312) 792-2700
▶ CIRCLE 629

▼ IGBT BUS BARS KEEP INDUCTANCE DOWN

Customer needs for a lower inductance power-distribution path to their IGBT modules is met by a line of IGBT bus bars. The bars provide the low-inductance characteristics needed for optimum operation of high-current modules. They consist of alternating copper plates (plus and minus bus) and specialized dielectric layers which are laminated into a multilayer power-distribution system. The wide copper plates act to cancel parasitic inductance and suppress transient voltages in the power circuit. Call for pricing.



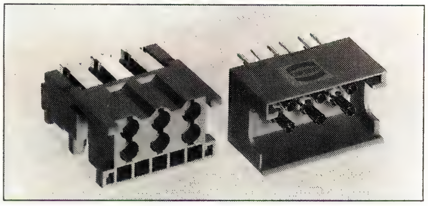
Eldre Corp.
1500 Jefferson Rd.
Rochester, NY 14623
(716) 427-7280
▶ CIRCLE 630

▼ RETENTION CLIP AIDS PLCC SOCKET

A retention clip is now offered for the low-profile, 32-position PLCC socket. The BA2651 clip is made from stainless steel and is well engineered for applications using high-G accelerated loading such as hand-held devices, which have been drop-tested from heights of 8 ft. The retention clip is used with Methode part no. 213-032-603. It has a locking mechanism and is removable.

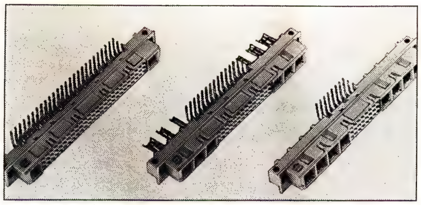
Methode Electronics Inc.
Interconnect Products Div.
1700 Hicks Rd.
Rolling Meadows, IL 60008
(800) 323-6864
▶ CIRCLE 631

NEW HIGH DENSITY MICRO-COAXIAL CONTACTS



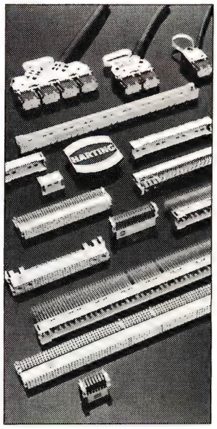
Designed for high speed data transfer rates. Can be used in the IEC 1076-4-2 2.5mm High Density connector system,har-pak ®. Provides more space efficiency, high frequency capability, easy handling, low applied cost and application with current equipment practice and emerging metric equipment practices. Designed for PCB termination on both daughtercard to backplane connection;allowing users to bring signal directly into the backplane without a cable transition.

CIRCLE# 160



COMPLIANT PIN DIN 41612-TYPE M INVERSE CONNECTORS

HARTING'S compliant pin Inverse Type M DIN 41612 Eurocard connectors allow-continued development of backplane technology using solderless termination and double-side surface mounting. Applications include telecom, medical and high speed computers. Connector-cavities accommodate the DIN 41626 high voltage, power, coaxial or fiber optic contacts. Connector arrangements can accommodate 2 to 10 special purpose contacts and 78 to 6 standard contacts respectively.Compatible with HARTING male press-in tooling without modification, it can be delivered with special press-in inserts to allow use of 'Flat Rock" or simple flatpress-in dies. **CIRCLE# 161**



har-pak® 2.5 MM High Density Connector system

Developed for backplane and daughterboard applications in modern rack systems. The 5 row 2.5 mm connector design offers solderless PCB terminations, optimum utilization of space, three dimensional modularity, high contact density, EMI protection, and the ability to double-side surface mount components on daughter cards without loss of a 15 mm card pitch. The har-pakconnectorsystempermitsusing athreedimensional2.5mmgrid.Withthe exceptional capabilites of the connector,onlyoneconnectorstyleisrequiredto solveyourpower,signal,ground,andhigh data rates; simplifying the design and manufacturing of future systems.The compliant pin technology utilizes the same 1 mm plated through hole standard for many DIN 41 612 compliant pin technologies. The consistency in design uses the many years of manufacturing and design experience already available.These attributes combined can lead to new advancements n board-level designs: 15 mm card pitch with double-sided surface mounted daughter cards, butterfly or mid-plane techniques, modular design both horizontally and vertically,low number of system components, combination with other standardized packaging systems,and lower applied costs.

CIRCLE# 162

'har-mik®', NEW MINATURE CONNECTORS FROM HARTING ELEKTRONIK

New, comprehensive range of miniature connectors, the 'Pin and Socket' I/0 connectors Series 60.01/02/03/04, are designed to meet the requirements of internal and external connections of the future.

- Reduced size: contact pitch of 1,27 mm
- High contact density: double standard D-Sub
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- Male and female IDC versions for discrete wire 28 to 30 AWG
- Male and female connectors wth straight and angled solder pins
- Many connector sizes: from 20 to 100 ways

CIRCLE# 163

DIN connectors

The Oscar for quality

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Die

DQS Deutsche Gesellschaft zur Zertifizierung
von Qualitätssicherungssystemen mbH

bescheinigt in Zusammenarbeit mit der

Vereinigung der Technischen Überwachungs-Vereine e.V. (VdTÜV)

hiermit, daß das Unternehmen

HARTING ELEKTRONIK GmbH
Geschäftsbereich Leiterplattensteckverbinder
Marienwerder Straße 3

D-4992 Espelkamp

ein

Qualitätssicherungssystem

eingeführt hat und anwendet.

Durch ein Qualitätsaudit der DQS wurde der Nachweis erbracht,
daß dieses Qualitätssicherungssystem die Forderungen der folgenden Norm erfüllt:

DIN ISO 9001

Qualitätssicherungssysteme
Modell zur Darlegung der Qualitätssicherung
in Design/Entwicklung, Produktion, Montage und Kundendienst
(identisch mit ISO 9001 : 1987, EN 29 001 : 1987, BS 5750 Part 1 : 1987)

Dieses Zertifikat ist gültig bis 20. Februar 1994

Zertifikat-Register-Nr.: 14 158-01/1

Frankfurt am Main, 21. Februar 1991

DQS Deutsche Gesellschaft zur Zertifizierung
von Qualitätssicherungssystemen mbH · Berlin

PRÄSIDENT

GESCHÄFTSFÜHRER

Geschäftsstellen: D-6000 Frankfurt 60, August-Schanz-Straße 21 A D-1000 Berlin 30, Burggrafenstraße 6

DQS, the German QA System Certification Company, has awarded our PCB Connector Division the DIN ISO 9001 Certificate. This confirms our efforts to achieve perfection in both products and manufacturing methods.

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READER SERVICE 159

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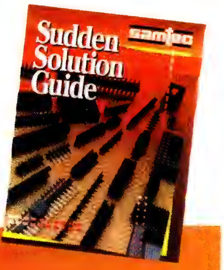

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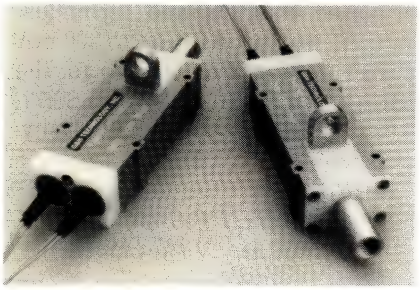
READER SERVICE 205

▼ CELL-BYPASS SWITCH PREVENTS POWER LOSS

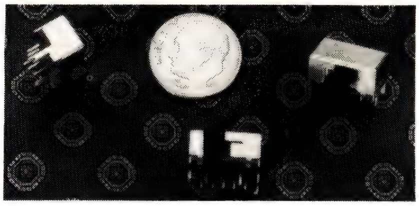
Highly reliable protection against complete power loss caused by failure of individual cells in series-connected batteries is provided by the model 1176 cell-bypass switch. The switch senses a cell failure and immediately and automatically opens an alternate current path, bypassing the failure and ensuring continued battery service. Typical pricing is $1950 in quantities of 50.



G&H Technology Inc.
750 W. Ventura Blvd.
Camarillo, CA 93010
(805) 484-0543
▶ **CIRCLE 632**

▼ SWITCH COMBINATION MARRIES ROCKER, SLIDE

The MPS Series switches pack a single-pole momentary pushbutton and a three-position slide switch with a common actuator in a tiny package. These right-angle, pc-board switches measure 0.512 in. long by 0.290 in. wide and project 0.256 in. above the pc-board surface. Three models comprise the series: the MPS101, an on-on-off slide configuration, and the MPS101A and 101B, two different on-on-on slide-configuration pinouts. Pricing for the MPS101 is $1.69 in lots of 1000.



MORS/ASC
134 Water St.
Wakefield, MA 01880-4444
(617) 246-1007
▶ **CIRCLE 633**

▼ SUBMINI PUSHBUTTONS FIT 22-MM CUTOUTS

A line of snap-in pushbuttons fits 22-mm panel cutouts. The MB Series switches come in single-, double, and four-pole configurations and with either momentary or alternate actions. Their slow-make, slow-break contacts inhibit sparking and increase their ac-operating life. Models with silver terminals are rated at 6 A at 125 V ac and 3 A at 250 V ac. Those with gold-plated terminals are rated at 0.4 VA maximum at 28 V ac/dc maximum. Call for pricing.

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
▶ **CIRCLE 634**

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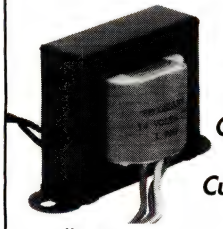

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READER SERVICE 137

SWITCHES & RELAYS

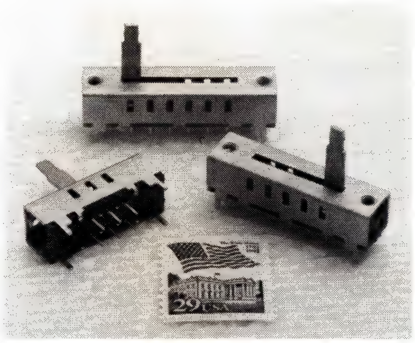
▼ SOLID-STATE CONTACTOR DISSIPATES LOW POWER

Less reliable mechanical contactors can be replaced with the KW Series solid-state contactors. Rated at 50, 500, and 1000 V dc with up to 250 A per pole, the contactors' maximum pole dissipation is 125 W with drops of less than 1 V. The units include the complete drive and protection circuitry. Only a single input-control signal (CMOS logic levels or a 5-V inverted open collector) is required. Load current is monitored in either direction by means of the company's current-sense techniques. Call for pricing and delivery.

Gentron Corp.
7345 E. Acoma Rd., Suite 101
Scottsdale, AZ 85260
(602) 443-1288
▶ CIRCLE 635

▼ SLIDE SWITCHES ARE WASHABLE

A line of multi-position, single-pole slide switches is designed for those applications where one of several single-pole on-off switches can be individually selected by positioning a sliding lever. The selected switch is turned on while the others are off. Three models are available: the MSL33 with three positions, the MSL55 with five, and the MSL66 with six. All are built with a phenolic laminated base and epoxy-sealed, silver-plated contacts and terminals. Contacts are rated for up to 200 mA at 125 V ac or 30 V dc. Pricing for the MSL33, MSL55, and MSL66 is $0.77, $0.91, and $1.02, respectively. Delivery is from stock.



MORS/ASC
134 Water St., P.O. Box 544
Wakefield, MA 01880-4444
(617) 246-1007
▶ CIRCLE 636

▼ DIP ROTARY SWITCHES AVAILABLE ON REELS

The ND3 Series DIP rotary switches are now offered in 22-mm-wide, 500-device tape-and-reel packages. In addition to the standard 330-mm reel diameter, 370-mm-wide reels are available to meet EIA requirements. The switches are rated at 100 mA at 50 V dc (non-switching) and 100 mA at 5 V dc (switching). Models can be specified with real or complement-coded circuits, decimal or hexidecimal positions, and screwdriver or shaft actuators. Call for pricing and delivery.

NKK Switches
7850 E. Gelding Dr.
Scottsdale, AZ 85260
(602) 991-0942
▶ CIRCLE 637

▼ AC SOLID STATE RELAYS SWITCH LOW POWER

Low-power ac switching applications are served by the C45 family of solid-state relays. The units are rated for load voltages up to 250 V ac rms from 40 to 440 Hz and are well suited for resistive and reactive loads with power factors as low as 0.2. They're designed to accommodate several different input-control requirements for maximum flexibility in socket support. Back-to-back silicon-controlled rectifiers and a patented zero-crossing circuit comprise the devices. Dielectric breakdown voltage is up to 4000 V rms. Pricing starts at $7.60 in prototype lots. Delivery is stock to 6 weeks.

Teledyne Solid State
12525 Daphne Ave.
Hawthorne, CA 90250
(213) 777-0077
▶ CIRCLE 638

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▼ SOLDER-PRACTICE KITS HELP CHECK EQUIPMENT

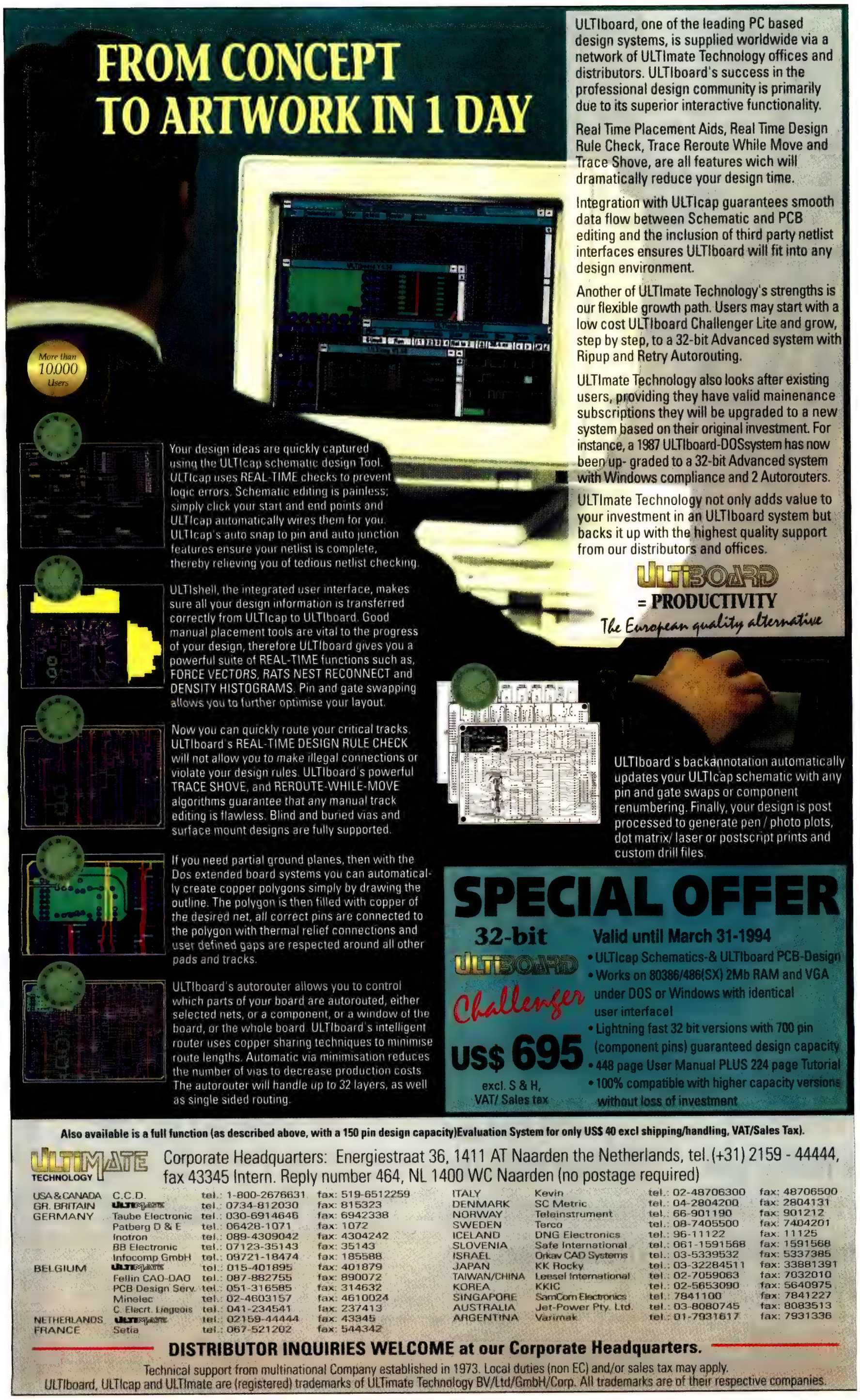
A line of 20 solder-practice kits addresses a variety of uses including operator training, machine diagnostics, stencil evaluations, speed checks, demonstrations, and experimentation. Most kits are available in quantities to build from 10 to 100 assemblies and in skill levels from beginner to highly advanced. The kits feature high-temperature Getek material equivalent to FR-5. Polyimide boards are also available. Standard for each SMT kit are double-sided boards measuring 5.5 by 4 in. with tooling holes. Three kits support a daisy chain ball-grid array package with 169 or 225 bumps on 1.5-mm centers. Prices run as low as $16 for through-hole kits with most SMT kits ranging from $22 to $50 each. in lots of 100. Delivery is from stock to 2 weeks.

TopLine
P.O. Box 5100
Garden Grove, CA 92645
(310) 433-7000
▶ CIRCLE 639

▼ HIGH FREQUENCIES WON'T DAUNT CIRCUIT MATERIAL

A circuit material for commercial applications offers improved electrical properties at high frequencies compared with FR-4-type circuit boards. The RO3003 material, which costs 25 to 30% less than competitive Teflon fiberglass materials, provides a uniform dielectric constant, low losses, stable performance over temperature, very good dimensional stability, and excellent plated-through-hole reliability. It's suitable for use in commercial wireless applications such as direct broadcast satellite receivers, cellular base-station power amplifiers, RF-identification systems, and personal communication systems. Initial offerings are in standard panels of 18 by 24 in.; in thicknesses of 0.010, 0.020, and 0.030 in.; and with 1/2 oz or 1 oz of electrodeposited copper. Call for pricing and delivery.

Rogers Corp.
Microwave and Circuit
Materials Div.
100 S. Roosevelt Ave.
Chandler, AZ 85226
(602) 961-1382
▶ CIRCLE 640



FROM CONCEPT TO ARTWORK IN 1 DAY

ULTIboard, one of the leading PC based design systems, is supplied worldwide via a network of ULTImate Technology offices and distributors. ULTIboard's success in the professional design community is primarily due to its superior interactive functionality.

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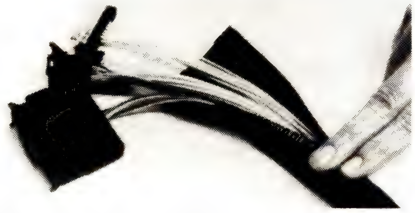

A protective outer sleeve with a wrap-on/-off closure design offers easy assembly and removal from cable harnesses. The Type XS500 removable braided sleeving is made with a hook-and-loop design that gives designers light weight, flexibility, and abrasion resistance. The sleeving is rated at 125°C with a temperature range of –40 to +125°C. It comes in glossy black and in six sizes. Small-quantity prices are from $1.93 to $4.30 per foot.

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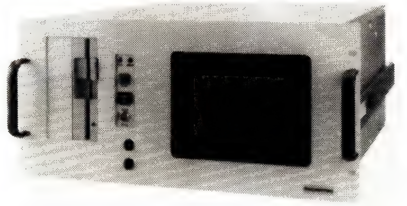

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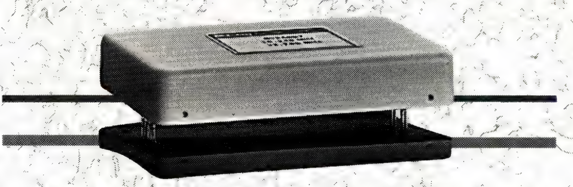

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▼ FIBER-OPTIC PRODUCTS FILL LARGE CATALOG

Catalog 82188 from AMP Inc. details a large selection of fiber-optic products including connectors, cables, LEDs, splices, tools and accessories, switches, couplers, splitters, attenuators, and more. Profusely illustrated with photos and drawings, the 204-page compendium contains complete specifications for all products. A reference section offers a treatise on fiber-optic technology as well as a glossary of terms. A listing of available detailed technical documents gives a further resource.

AMP Inc.
P.O. Box 3608
Harrisburg, PA 17105-3608
(800) 522-6752
▶ **CIRCLE 644**

▼ POTS, TRIMMERS IN FULL-LINE GUIDE

An assortment of sensors, trimmers, dials, single- and multi-turn potentiometers, and switches are offered in Catalog No. 529 from Spectrol. The catalog includes full engineering information as well as an informative description of the company's capabilities in designing custom products. Photos, dimensional drawings, and complete specifications are included for all products. Also offered is ordering information as well as a useful chart comparing the performance of different resistive elements.

Spectrol
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Ontario, CA 91761
(909) 923-3313
▶ **CIRCLE 645**

▼ HYBRIDS BROCHURE OUTLINES BENEFITS

Beginning with a general description of hybrid circuits, RCD Components's Hybrids brochure helps the engineer decide whether a hybrid implementation is right for his or her circuit. Design criteria are spelled out, as are the feasibility standards which determine whether a hybrid is the best solution. A section on protection and packaging describes options for physical protection of hybrids.

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Manchester, NH 03109-1824
(603) 669-0054
▶ **CIRCLE 646**

▼ SOLUTIONS GUIDE HELPS COMPONENT USERS

One of the industry's broadest ranges of components is showcased in a catalog that features helpful application information. Bourns's Solutions Guide RC3 stretches over 316 pages and covers the company's trimmers, resistor networks, switches, encoders, panel controls, dials, precision potentiometers, and transducers. One example of an application section is a designer's guide to trimmers that discusses operation theory and includes helpful definitions of terms. Information on assembly processing helps determine whether the devices are good for a given application.

Bourns Inc.
1200 Columbia Ave.
Riverside, CA 92507-2114
(909) 781-5500
▶ **CIRCLE 647**

▼ SMD CATALOG SPORTS PASSIVE, ACTIVE PARTS

A diverse range of surface-mounted products ranging from monolithic ICs, transistors, and diodes to LEDs, resistors, and capacitors is included in ROHM's 1994 SMD catalog. Thousands of part numbers are contained in the arrays of specification tables contained within the catalog's 168 pages. Dimensional diagrams are offered as are packaging specifications and examples of product designations.

ROHM Electronics
3034 Owen Dr.
Jackson Business Park
Antioch, TN 37013
(615) 641-2020
▶ **CIRCLE 648**

▼ CRYSTAL OSCILLATORS IN INFORMATIVE BOOKLET

Data clocks and crystal oscillators, both voltage- and temperature-controlled, are featured in a 26-page catalog. A broad range of clocks are covered, including surface-mounted types, CMOS/TTL versions, high-speed devices, models with tight stabilities, and dual baud-rate generators. A similarly wide assortment of crystal oscillators includes surface-mount types as well as dual-polarity and high-frequency types. Sections on environmental and mechanical specifications round out the catalog along with material on solderability and dimensional data.

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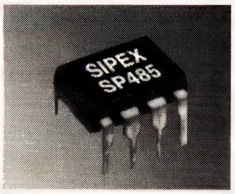

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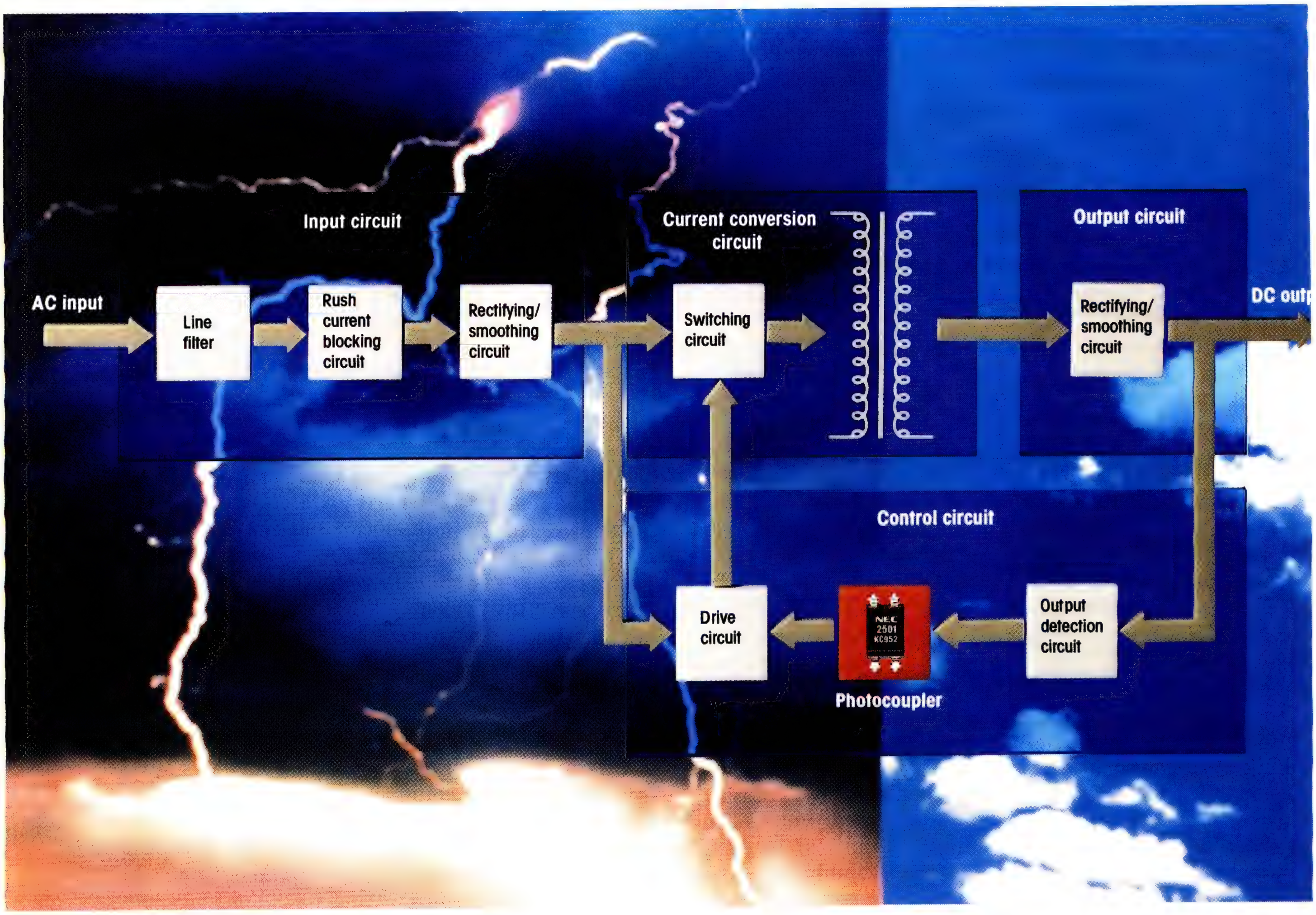

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PARALLELISM PUSHES DSP THROUGHPUT

A PARALLEL-PROCESSING DSP IC TAKES AIM AT MULTIMEDIA, DELIVERING 2 GOPS WITH FOUR 32-BIT DSP ENGINES PLUS A RISC CPU.

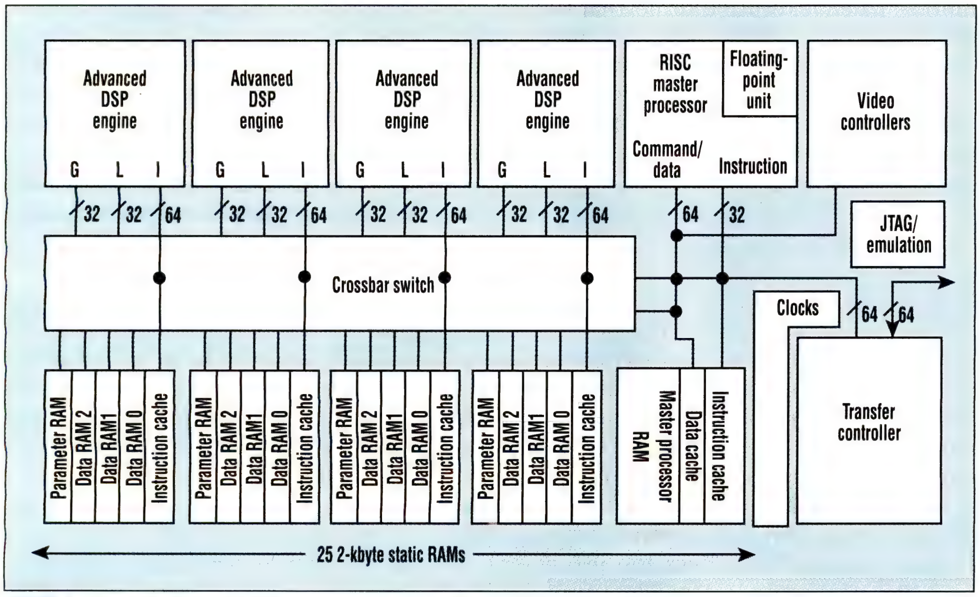
DAVE BURSKY

As users embrace the concept and compelling benefits of multimedia applications, many discover that most computers are either too slow or too costly. To improve system performance, higher-throughput processors are needed just to handle the computations in more complex applications and to control data flow. But that's only the first step. Image and audio processing also is being done by dedicated chips to offload the host processor.

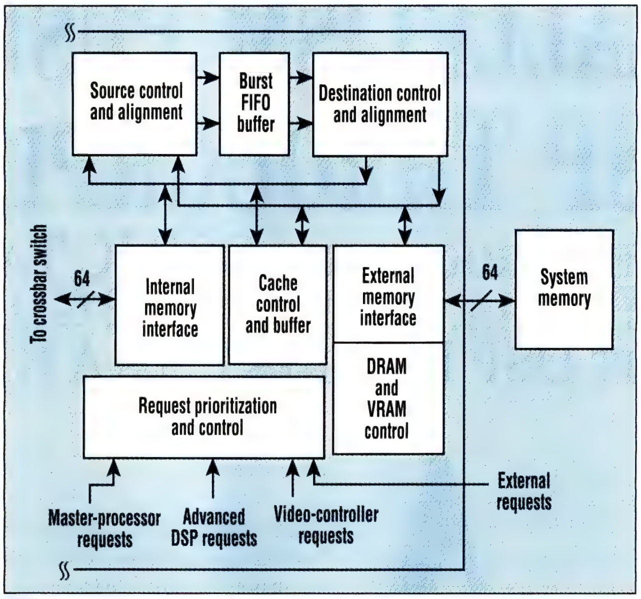
Although dedicated image-compression/expansion processors and separate audio-channel support can greatly improve performance over software-only image manipulation, they have their drawbacks. Today's silicon support typically consists of processors dedicated to each task—one for image compression/expansion, one for audio, another for a fax/modem, etc. These blocks are only loosely coupled to each other, which makes it difficult to coordinate activities and optimize operations. Moreover, many of the chips execute fixed, or only partially programmable algorithms to implement the desired function, which also limits system flexibility. Updates of improved algorithms would require chip replacements rather than just a software download if the processors were fully programmable.

Designers at Texas Instruments now hope to restructure the way systems are designed. They've collected all of the image, audio, and other digital-signal-processing functions together on one high-performance DSP chip. This "super" DSP chip can simultaneously process image, audio, and other signal-processing related data. The TMS 320C80 multimedia video processor (MVP) delivers close to 2 billion operations per second and can execute many of its processing functions in parallel. Key to the chip are its four independent and totally programmable DSP cores, a 32-bit RISC processor, and a floating-point coprocessor *(Fig. 1)*.

Each of the four 32-bit



1. WITH FIVE SEPARATE 32-BIT PROCESSORS on one chip, the multimedia video processor (MVP) developed by Texas Instruments can perform 2 gigaoperations per second and thus handle many real-time imaging applications. Four of the on-chip processors are high-performance DSP engines and the fifth is a 32-bit RISC CPU. All of the processors are interconnected to 50 kbytes of on-chip static RAM through a high-bandwidth crossbar switch. An intelligent controller transfers data at high speeds via DMA operations between the main memory and the on-chip SRAMs.


Source control and alignment
Burst FIFO buffer
Destination control and alignment
To crossbar switch
64
Internal memory interface
Cache control and buffer
External memory interface
64
System memory
DRAM and VRAM control
Request prioritization and control
External requests
Master-processor requests
Advanced DSP requests
Video-controller requests

2. THE INTELLIGENT transfer controller on the MVP chip handles data movements between the internal crossbar switch and the off-chip system memory. Because the control logic can support external DRAMs, VRAMs, static RAMs and ROMs, system designers can take advantage of the most cost-effective solution.

DSP blocks includes hardware to support multiplication-intensive signal processing, bit-field-intensive pixel manipulations, and bit-field-intensive entropy encoding/decoding (for example, Huffman encoding for facsimile). The MVP's 32-bit RISC processor contains an IEEE 754-compatible 100-MFLOPS floating-point unit that will support 3D computations, such as ray tracing. Also on the chip are a high-performance transfer controller and a dual video controller that supports a pair of simultaneous video-data streams (typically one for input capture and one for output display).

The MVP executes over 2 billion operations/s when clocked at 50 MHz. Each DSP block rips through up to 50 million instructions/s (each instruction can contain multiple operations). The RISC processor, the floating-point unit, and the transfer controller deliver the balance of the performance. With such an overall throughput, the chip can tackle many real-time multimedia applications—video conferencing, image compression/expansion for MPEG 1 or 2, video servers, X-terminals, 3D graphics, document image processing, etc. (the chip's first release, however, will operate at 40 MHz, which decreases the overall throughput by 20% but still gives it plenty of horsepower to handle current applications).

Because the processors all work in parallel and are independently programmable, the processing task at hand can use one or more DSP engines to process the data. Engines not needed for one task can be assigned to another. Thus, when the software is properly tuned, the chip will be able to multitask and simultaneously perform as a fax subsystem, an MPEG player with audio, etc. One MVP could perform the work of as many as 10 previous-generation DSP chips, simplifying overall system design.

Programming the parallel operations is simplified thanks to a full suite of software tools developed by TI. Designers will be able to work with assemblers, C compilers, and a novel algebraic assembler that supports the many different operations performed by DSP engines. Both software-simulation and hardware-emulation tools also are available. Those tools share the same graphical interface. A resident executive kernel that runs on the RISC engine supports multitasking and intertask synchronization and communications. Under the executive, tasks running on the RISC processor issue commands that are carried out by the DSP engines.

To hold the large amounts of data and instructions needed for each processor, 50 kbytes of static RAM are included on the chip. That memory is interconnected to the four DSP blocks through a crossbar switch that lets all the processors simultaneously access memory over their dual 32-bit data buses and 64-bit instruction bus. The processor also can simultaneously access its memory—a 32-bit-wide instruction cache and a 64-bit-wide data cache. That gives the processors an aggregate internal data-transfer rate of 2.4 Gbytes/s, an instruction-transfer rate of 1.8 Gbytes/s, and an off-chip data-transfer rate of 400 Mbytes/s (over a 64-bit data bus).

The on-chip memory is organized as a bank of 25 SRAMs, each 2 kbytes deep. Each of the four DSP blocks thus has five 2-kbyte SRAMs for its own use—one 2-kbyte section serves as a 64-bit-wide instruction cache, three sections are for data storage, and one stores parameters. The RISC engine also contains five SRAM blocks, but it groups them to form 4-kbyte-deep instruction and data caches and a 2-kbyte shared memory that only the RISC engine or the transfer controller can access.

The transfer controller performs autonomous DMA operations to rapidly transfer packets of data to or from the on-chip memory. Packet transfers include instruction- and data-cache servicing plus more complex, programmable, byte-aligned array transfers that can include X-Y or linear addressing of the source or destination array. The transfer controller processes source- and destination-addressing data with independent subcontrollers. It also has a burst FIFO buffer that supports DRAM page and burst modes, and buffers byte-misaligned accesses for more efficient accessing *(Fig. 2)*.

Furthermore, the transfer control block contains timing and address multiplexing control for off-chip DRAMs, video RAMs, SRAMs and ROMs. Data moves over a 64-bit data bus at up to 50 Megatransfers/s. A separate 32-bit address bus gives the MVP a 4-Gbyte address space, needed to handle the large image files common to multimedia applications.

Supporting DRAMs is relatively new for DSP chips because DRAMs typically couldn't keep up with the short bus cycles of a DSP chip. With the MVP, the multiple on-chip data banks basically perform like a level-one cache fed by the off-chip main memory. Because the image and multimedia files are usually very large, the need for low-cost but high-capacity memory pushed the DSP designers into including DRAM support.

The 32-bit RISC master processor, which coordinates all of the activities of the DSP chip, was designed to be programmed using high-level languages. The processor's integer por-

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tion employs a 32-bit instruction word and executes most register-to-register or load/store instructions in a single cycle. For higher-precision computations, the companion IEEE 754-compatible floating-point unit delivers 100 MFLOPS of peak throughput and can initiate a new floating-point addition or multiplication every cycle.

To maximize CPU performance, the 32-bit register file uses a scoreboarding approach to keep track of floating-point results and memory-load operations. That allows the master processor to continue execution and only stall if an instruction tries to use a register before the prior operation loads its result. A three-stage pipeline is used by the master processor, and a new instruction execution starts every cycle (assuming no stall condition is detected). The cache control dedicated to the RISC processor manages both the instruction and data caches. When a miss occurs, the cache control requests a cache line fill from the transfer controller, which then transfers a packet from main memory.

The MVP's definition was driven by three areas: manipulating data for image processing and recognition, video and still-image compression, and high-performance computer graphics. These areas all share the need for multiplication-intensive algorithms that perform convolution and frequency-domain transforms. Also, both compression standards and graphics rendering need pixel and bit-field processing. However, most previous DSP chips weren't very good at processing bit fields and multiple-pixel quantities.

To meet those needs, the advanced DSP blocks on the MVP use a different hardware approach and a different instruction set than what's normally found on older DSP ICs. Because the international video and still-image standards require discrete-cosine frequency transforms (DCTs), particular attention was paid to the MVP's DCT performance and precision. However, although massive processing is required, 16-bit or less fixed-point multiplications with 32-bit accumulation usually suffices.

That observation led to an unusual design of the ALU in the TMS-320C80's DSP engines. Rather than use a 32-bit ALU for everything, an ALU was created that could be split into two 16-bit ALUs, or even into multiple 8-bit ALUs. Subdividing the ALU into as many as four smaller ALUs allows many byte-wide operations (character or pixel manipulations) to be done in parallel. If all four DSP engines are used in parallel to process pixel data, sixteen 8-bit pixels per cycle could be processed.

One 64-bit-wide instruction word controls each DSP block. The word contains fields that independently control the data unit with its multiplier and data path, and the two address units. As a result, all sections of the DSP engine can operate in parallel—simultaneously executing data fetches, next-address generation, arithmetic operations, and so on.

The instruction fetches and the instruction cache are controlled within each DSP engine. Instructions are executed in a three-cycle pipeline, with a new instruction starting every cycle (assuming no stalling condition occurs). If a cache miss occurs, the cache controller makes a packet request to the transfer controller, which will then transfer a new sub-block into the cache.

Each DSP engine includes a register file with 44 user-visible general-purpose registers that can be arranged into files based on the register's functions. Most of the registers also allow more than one access in a cycle, with some in the data unit allowing over 10 accesses in one cycle. The data unit contains the data registers, a 16-bit multiplier, and the ALU data path.

The multiplier can perform one 16-bit-by-16-bit or two 8-by-8-bit multiplications in one cycle. It also has a rounding option that was a direct result of maintaining the specified accuracy for the video-compression standards. The data path contains a barrel rotator, a mask generator, a 1-bit-to-n-bit expander (useful for binary to color transformations), and a three-input ALU that can combine the mask or expander output with register data to create over 2000 different processing options. Each DSP block also includes two address units that can operate in parallel to control load or store operations with on-chip RAM.

With each instruction performing many operations in a single cycle, it was imperative to make the looping very efficient. To do that, each DSP engine includes three zero-overhead loop controllers. Therefore, even nested loops can be handled rapidly. Each loop controller has a set of registers that specifies starting and ending addresses, and current and initial loop counts. The loop controllers can also be used to perform zero-overhead branches to a run-time patch in code segments. Because the loop-control registers are in the register file, the results can be written to the loop-count register to control whether or not a branch is taken, based on a zero result.

The MVP was designed with multimedia applications in mind, not surprising , it includes not one, but two independent video ports. Each port's logic includes all of the video timing circuits and registers needed to control horizontal and vertical synchronization and blanking timing, as well as support a two-dimensional border region. The ports are independent, each with its own asynchronous clock input. Consequently, one could be used as an input-capture port and the other as a video output port, or both can be used as inputs or outputs simultaneously.

The complexity of the MVP probably makes some system designers nervous when it comes to verifying system operation. To assuage most of these concerns, about 10% of the transistors used in the non-memory logic were devoted to test logic. The chip includes a joint-test-action-group (JTAG) test port to allow for thorough testing. Also, all storage nodes on the chip can be loaded or read so that boundary-scan testing can be done. Other features in the scan path support emulation loading and dumping of the MVP's internal state. Address comparators were also added to support breakpoints. ☐

PRICE AND AVAILABILITY

The TMS320C80 multimedia video processor comes in a 305-pin ceramic pin-grid array and is available in sample quantities. In lots of 10,000 units, the MVP will sell for between $300 and $400. Availability of production quantities is scheduled for early 1995.

Texas Instruments Inc., Semiconductor Group, SC-94008, Literature Response Center, P.O. Box 172228, Denver, CO 80217; (800) 477-8924, ext. 4500 (for literature); (214) 644-5580 (for technical questions). **CIRCLE 511**

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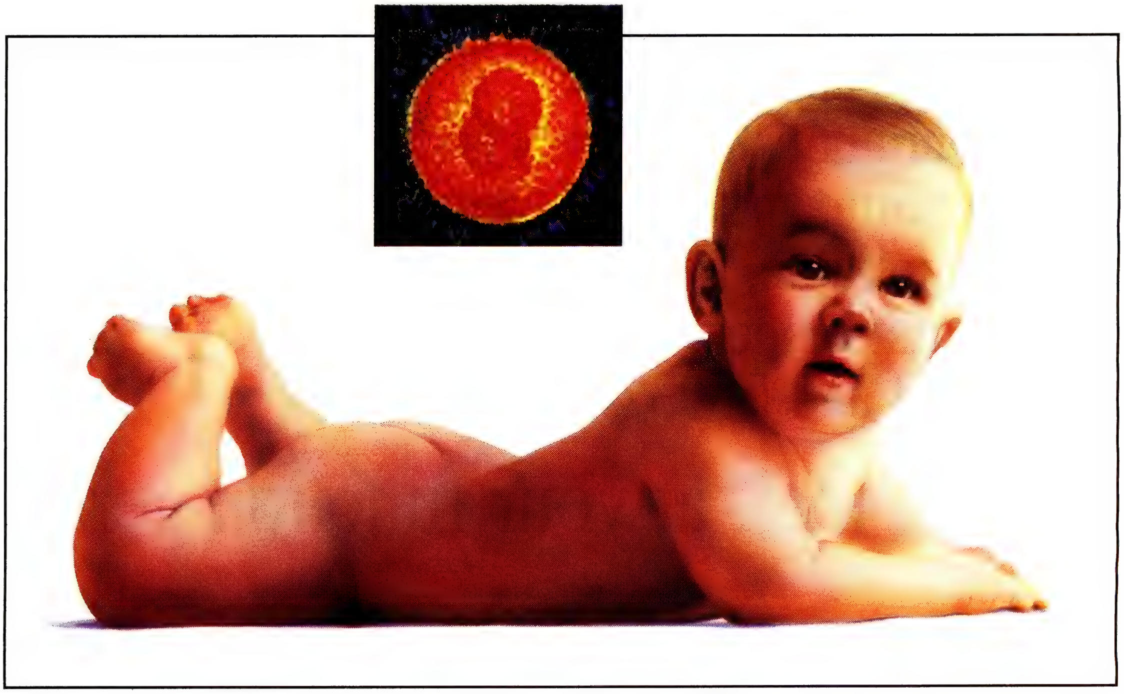

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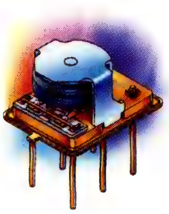

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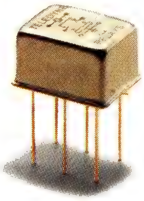

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PORTABLE WORKSTATION RETAINS DESKTOP SPECS

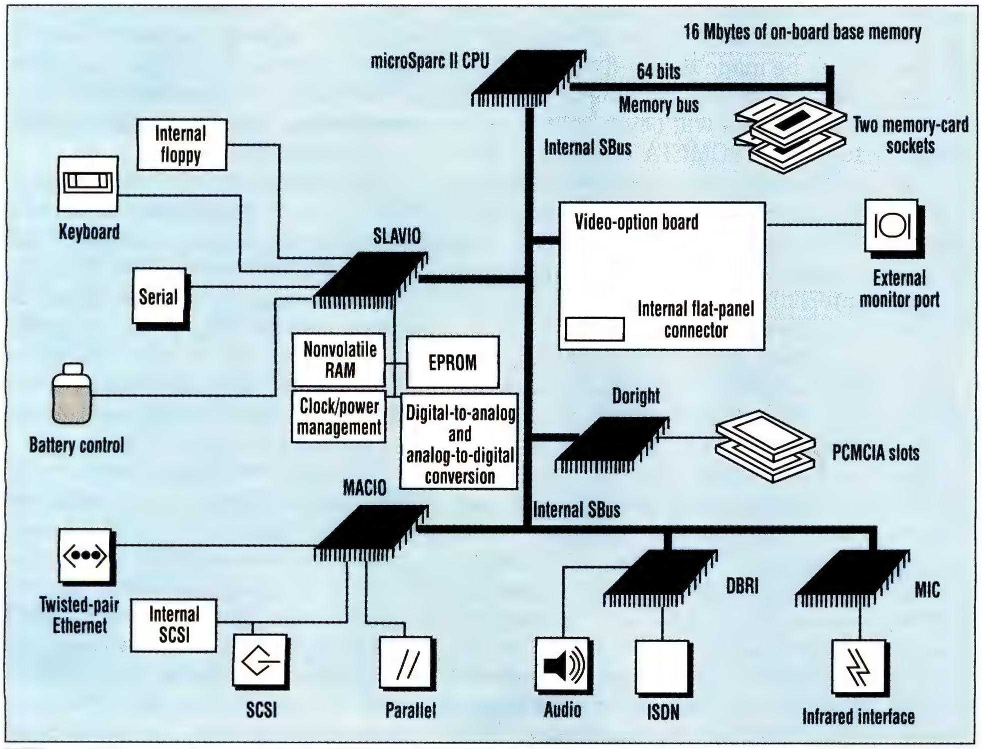
HIGH-PERFORMANCE AND FULL-FUNCTION NETWORKING CAPABILITIES ARE BUILT INTO A ROVING 12-LB. SPARCSTATION.

RICHARD NASS

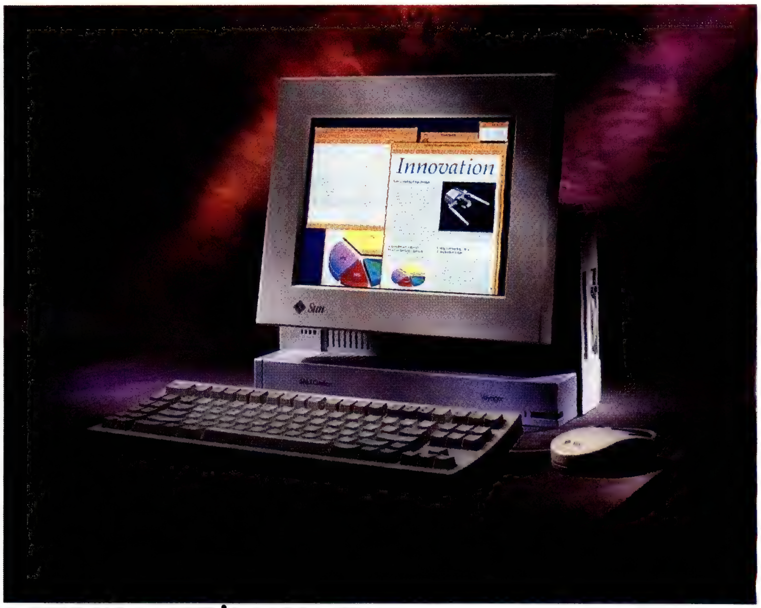
Workstations have sat on designers' desks for many years, traditionally being tied into a network where the engineer can pull down an application, store files, and send and receive electronic mail. But the days of an engineer remaining in one place are numbered, with engineers travelling to customer sites or other company offices. That means leaving the applications and data behind. If engineers could bring these workstations with them, though, their everyday tasks could be streamlined.

Such portability is possible with the Voyager workstation designed by Sun Microsystems Computer Corp., Mountain View, Calif. Built with an emphasis on networking, it's a complete Sparcstation, but in a portable package. Says Greg Munster, product-line manager for nomadic computing at Sun, "We see the networking capability as a critical element for this product, because no matter how much performance and capability you can pack into a machine, you still need the ability to tie it in to other systems." Ideally, network access must be easy and user transparent.

The networking aspects include how applications are accessed and how communications occur with other



1. THE MAIN COMPONENTS OF THE VOYAGER, including the CPU, communicate over an internal SBus. The MACIO and SLAVIO chips handle most of the I/O, while the DBRI chip supplies the 16-bit audio and ISDN capabilities. The MIC chip acts as an SBus-to-IR interface. The Doright interface chip is an SBus-to-PCMCIA adapter.



2. THE VOYAGER'S DISPLAY rises vertically from the base. The system measures 14 by 5.5 by 15 in., and weighs about 12 lb. Sun claims that the system meets or exceeds a typical Sparcstation in performance, display capabilities, and memory expansion.

systems. The company claims that the most popular applications on a Sun workstation are communications packages, such as E-mail or group calendaring. The network link also has access to other networks, including the Internet.

The Voyager's basic architecture consists of three pc boards: the main CPU board, a frame-buffer daughtercard that plugs into the CPU board, and a small I/O board that the main CPU board plugs into. This design is similar to the company's SparcClassic. It contains the main CPU board and an I/O board that holds the routings and connectors.

Generally, Sun systems employ a frame-buffer card that connects to the 32-bit SBus. An exception had to be made for the Voyager because more video functionality was required. It also passes some video signals back through the CPU board to a video-output connector on the back of the machine, a feature needed to drive an external display.

The CPU board is built with an internal SBus, although the system contains no SBus expansion slots. All of the Voyager's subsystems hang off the internal SBus. A microSparc II processor, the latest in the microSparc family, functions as the machine's engine. The CPU's 60-MHz clock frequency puts the system in the mid-40 SPECmark range. By comparison, the SparcStation LX and SparcClassic are each built with the previous-generation microprocessor, which offers about half the performance. The microSparc II was designed by Sun and is manufactured by Fujitsu.

The CPU, along with five other key ASICs—the MACIO, SLAVIO, DBRI, MIC, and Doright chips, communicate over the SBus *(Fig. 1)*. The MACIO and SLAVIO chips are Sun's basic master and slave I/O interfaces. These permit access to the SCSI, parallel, and other I/O interfaces. The dual basic-rate interface (DBRI) chip from AT&T supplies 16-bit, CD-quality stereo audio and ISDN capabilities. The Sun MIC chip acts as an SBus-to-IR interface, allowing the Voyager to operate as a server to "infrared-literate" devices like PDAs and notebook computers. The interface employs the Hewlett-Packard SIR infrared protocol, and is also compatible with the Sharp-Apple protocol. Sun's Doright chip is an SBus-to-PCMCIA adapter. It's an interface to two Type I or II form-factor cards or one Type III card.

Because no SBus slots are on the Voyager, any external expansion must be made through the PCMCIA slots. With the introduction of this system, Sun will begin rolling out a family of PCMCIA cards. The first will be a 14.4-kbit/s modem (supplied by US Robotics on an OEM basis). This standard modem, which was customized for the Voyager, had its internal buffers quadrupled in size to increase performance.

Although no other PCMCIA cards are currently available, Sun is working with key vendors to produce cards, such as a token-ring interface or a serial-port card. Sun also offers a PCMCIA developer's kit that supplies the tools and components necessary for OEMs to develop custom products. PCMCIA was adopted as a way to plug in a modem. "A year ago, we probably would have just built a proprietary modem and dropped it into the machine rather than employ the PCMCIA interface," says Munster. In addition to the modem, users will receive a driver that lets them connect a second serial or flash-memory card. In addition, the operating system will support PCMCIA modems, flash-memory devices, and ATA-based mass-storage cards.

The CPU board contains all of the processing functions except the video. Due to the lack of video processing, Sun offers various display options. By making the video board a plug-in module, it supplies a degree of flexibility. As display technology progresses, upgrades will be relatively easy to perform.

There are currently two video options: pure monochrome to drive a monochrome flat-panel display; and an accelerated color display that employs the company's Turbo GX accelerator chip to supply 8-bit accelerated graphics on a color flat-panel LCD. The Voyager also supports any standard external color monitor and can drive a projection system.

Because the base memory (16 Mbytes) for the system is soldered onto the back of the CPU board, there's no zero-memory configuration. In addition, the board has two memory-card slots, but they aren't SIMM types. The memory cards are similar in form-factor to PCMCIA cards, except that the connector is on the card's long edge. The cards come in 16- and 32-Mbyte densities. As a result, the Voyager's maximum memory configuration is 80 Mbytes, using two 32-Mbyte cards plus the

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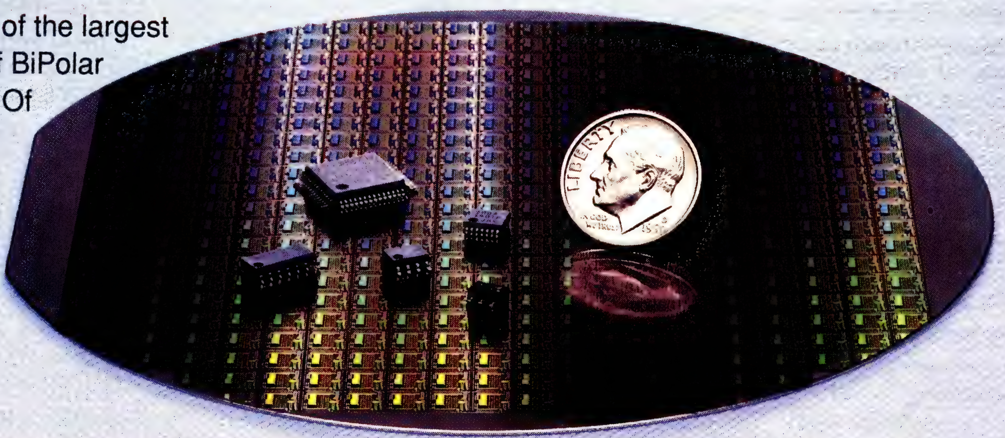

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NJU3714	12-bit Serial In Parallel Out with Cascade Function	D, G20
NJU3715	16-bit Serial In Parallel Out	L, G22
NJU3716	16-bit Serial In Parallel Out with Cascade Function	L, DMP24
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standard 16 Mbytes. The cards are user-upgradable: Users simply remove the system's back panel and plug the cards into the CPU board.

One design objective concerning the Voyager was to maintain the capabilities of a Sparcstation workstation, meeting or exceeding a typical Sparcstation in terms of performance, display capabilities, memory expansion, and so on. A second goal was to address the system's ergonomics. The machine had to be physically small, light in weight, and convection-cooled (needing no fan). Moreover, the Voyager employs a high-resolution active-matrix LCD, which like all flat-panel displays, has very little screen flicker.

The monochrome display features a resolution of 1152 by 900 pixels and a measures 14-in. diagonally, which, according to Sun, makes it comparable to a 16-in. CRT (flat-panel displays make greater use of the entire screen for viewing than CRTs). The color display has a 1024-by-768-pixel resolution and a 12-in. diagonal measurement. Both LCDs offer 106-dot/in. resolution.

The Voyager is built with a Toshiba 340-Mbyte, 2.5-in., hard-disk drive, the first time Sun has used this form-factor drive. The 2.5-in. drive is becoming more viable as its capacities increase. Samples of 740-Mbyte, 2.5-in. drives are already beginning to appear. Also included in the Voyager is Sun's standard 3.5-in., triple-density, floppy-disk drive. This drive is compatible with standard drives, allowing files to be transferred from DOS-based machines.

The system can be expanded: A look at the back panel reveals all of the ports a user would expect to see on a Sparcstation, with one exception. The Ethernet interface only accepts twisted-pair wires. In the past, Sun employed an access-unit interface (AUI), but this system does not for several reasons. First, it requires a physically large connector that's difficult to squeeze onto a small system. Second, the AUI requires about 5 W of power. This isn't viable on a battery-powered portable system. Third, Sun feels that the user base is moving toward twisted pairs.

Energy efficiency also was a design focal point. The system's power-management chip (PMC) can transparently shut off everything in the system, including the microprocessor, which has built-in idling capabilities. The CPU itself consumes 5 W, but can be idled during normal operation and brought back to full speed very quickly. The Unix idle loop accomplishes this by powering the system down instead of just executing "no ops." When an interrupt occurs to bring the system out of the Unix idle loop, the CPU is fired up. In the idle mode, the power consumption is reduced by 90%.

A lithium-ion battery is employed that offers a higher energy density than traditional NiCd or NiMH batteries. The 40-Wh battery offers about 2 hours of average use. Its recharge time is approximately 1.5 hours. In addition, the lithium-ion battery has more "intelligence" than NiCd batteries. For example, it provides a high degree of predictability in terms of remaining battery life. Users can activate a software tool that accurately predicts how much time and battery life remain.

The system's standard configuration holds an internal ac power supply that sits in the foot of the machine. Because the power supply and battery have identical footprints, the power supply can be swapped with the battery to take the system on the road. In this case, the power supply can operate either outside the machine to recharge the battery or from an ac source. In the latter configuration, the machine is powered from the ac source while the battery is being trickle-charged.

An integrated power-management tool gives users some flexibility in terms of how the system is powered down. It allows them to set the power-down interval for the hard-disk drive and display backlight when there's no user activity.

Power savings also comes from the convection cooling employed because there's no fan. On top of that, the thermal-management system inside the box is an aluminum frame which offers a high level of structural strength, further facilitating heat distribution. To minimize hot spots, all of the boards are coupled to this frame both mechanically and thermally, supplying uniform heat distribution. The convection cooling operates with the chimney effect, where the base and the top of the CPU are ventilated for natural cooling.

The Voyager fits in a sleek and compact package, with its base measuring 14 by 5.5 in. The flat panel rises vertically about 15 in. from the base *(Fig. 2)*. The detachable keyboard with full-size and full-travel maintains all of the functionality of a standard Sparcstation keyboard in a space approximately 5 in. shorter and 1 in. narrower. Users can opt to employ the standard Sparcstation keyboard as well. Total system weight is 12 to 13 lbs., depending on the display and keyboard.

The Solaris 2.3 operating system ships with the Voyager. Within the operating system is a point-to-point protocol that lets the system run the full TCP/IP networking suite over either a standard telephone line, an asynchronous analog line, or an ISDN connection (ISDN is built into the Voyager). An analog modem also is available as an option. The operating system supports three modes—standard, disconnected, and remote. A bundled mail tool, which sorts and spools mail, supports all three modes. The default installation of Solaris requires less than 100 Mbytes, but it can be customized by adding documentation, for example, which could add another 60 Mbytes.

Other software capabilities include a suspend-resume feature. When the suspend mode is enacted, the system state is stored in nonvolatile memory in a disk partition. Upon resuming operation, all of the processes are restored from that partition and users are brought back to the same point that they left without the long bootup delay.☐

PRICE AND AVAILABILITY

The Voyager, available now, ranges in price from about $10,000 to $15,000, depending on the display choice and memory configuration.

Sun Microsystems Computer Corp., 2550 Garcia Ave., Mountain View, CA 94043; (415) 960-1300. **CIRCLE 512**

HOW VALUABLE?	**CIRCLE**
HIGHLY	533
MODERATELY	534
SLIGHTLY	535

PRODUCTS NEWSLETTER

SAMPLES AVAILABLE FOR MODULAR ATM ICs

Fujitsu Microelectronics now has sample quantities of its family of ATM transmission and switching products. The chip set can support the three-layer ATM protocol. The straightforward separation of functions between chips permits numerous configurations used in node applications (such as workstation adapter cards), as well as in the design of hub/router products. The Adaptation Level Controller (ALC) chip performs segmentation and reassembly (SAR) on incoming and outgoing data, with an ability to create up to 1024 virtual circuits per port. The chipset's Network Termination Controller (NTC) provides ATM cells with access to the physical layer, translating between ATM and several protocols, including SONET 1/3, DS-3, and E-3. A 4-by-4 Self Routing Switching Element (SRE) can be cascaded for expansion up to a 64-by-64 matrix. At the heart of the routing scheme, an Address Translation Controller's proprietary interface makes it possible for the SRE to receive routing information generated by the NTC in a 3-byte routing tag transmitted between ATM cells. Samples/production pricing are: SRE, \$210/\$75; NTC, \$170/\$75; ALC, \$210/\$105; ATC, \$130/\$45. Contact Fujitsu at (408) 922-9000. *LG* CIRCLE 686

INTERFACE SIMPLIFIES VERILOG CODE CHECKER

A graphical user interface added to version 2.0 of the Verilint Verilog code purifier from interHDL Inc., Sunnyvale, Calif., makes it easier to check designs for syntax and semantic errors. Users select various parts of a design, run Verilint to detect errors, edit the source code to correct errors, and re-run Verilint until all errors are removed. Source code is displayed in a text window, and errors and warnings in an error window. Verilint also highlights the error location in the source code for an easier and faster correction cycle. The new graphical interface includes a toolkit that supports a text editor, a hierarchy browser, and a pretty printer. The hierarchy browser, which is used to navigate through the design, displays both module and instance hierarchy. In addition, the Veriframe project- and tool-management framework provides a graphical front end for managing multifile designs and for invoking specific tools. Verilint runs on Unix workstations. Pricing starts at \$2000 for single-user licenses. Call (408) 749-8775. *LM* CIRCLE 687

SOFTWARE EXPLORES DESIGN SERVICEABILITY

A new analysis program from Boothroyd Dewhurst Inc., Wakefield, R.I., provides a systematic, quantitative way to determine the serviceability of a product at the conceptual stages of design. Version 1.0 of the Design for Service (DFS) software works with the company's Design for Assembly tool to analyze critical assembly information and generate DFS reports. By integrating the two products, important manufacturing data, such as parts consolidation responses, parts lists, and assembly times and costs, are available without gathering new information. Users need only identify each service item and choose a disassembly sequence. A re-assembly sequence is automatically generated by the tool. Using specialized DFS databases, a finished analysis provides a worksheet of service tasks with estimates of total disassembly and re-assembly times, a serviceability rating index, and critical identification of serviceability costs. DFS Version 1.0 runs on PCs under Windows. Call for pricing and more information. *LM* CIRCLE 688

UPGRADED MACH FAMILY PLDs RUN AT 133 MHz

Thanks to a tweak in its CMOS process, Advanced Micro Devices Inc., Sunnyvale, Calif., has pushed the internal clock speeds of its Mach family of complex programmable logic devices up to 133 MHz for the Mach210A-7, and up to 100 MHz for the larger Mach230A-10. The chips, which contain approximately 1800 and 3600 gates, respectively, also have pin-to-in propagation delays of 7.5 and 10 ns, worst case—a 25% improvement over previous family members with identical complexities. The Mach210A-7 and the 230-10 also support system-level clock speeds of up to 100 MHz and 80 MHz and contain 64 and 128 macrocells, respectively. The short propagation delays readily allow the fast chips to operate in high-performance systems that employ Intel's Pentium or the IBM/Motorola PowerPC processors, as well as other high-speed CPUs. The Mach210A-7 comes in a 44-lead package that allows for up to 38 inputs or 32 outputs; the 230A-10 comes in an 84-lead package and has up to 70 inputs or 64 outputs, including four global clock lines. In lots of 1000 units, the 201A-7 and 230A-10 sell for \$10.75 and \$75, each, respectively. Call (408) 987-3100. *DB* CIRCLE 689

Edited by Clifford Meth

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Mike Quinlan, Chairman, CEO McDonald's (left)

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SMART FLASH MODULE REPLACES EEPROMS

With capacities of 256 kbits to 8 Mbits, a smart flash-memory based module—the ES1016 series—can directly drop into EEPROM or flash-memory-based sockets. Developed by Eurom, it can replace more costly EEPROMs, while delivering four times the capacity for about the same price. It can also be programmed via a serial port.

Although the module uses 34 pins instead of the 32 pins typically used by the byte-wide flash and EEPROM-based non-volatile memories, all but the upper two pins on the DIP-style package (pins 1 and 34) match with pins already used by the other byte-wide memories. The two additional pins provide the serial data input and output lines. An adapter socket developed by Eurom drops into 32-pin sites and provides connection points for the two extra pins.

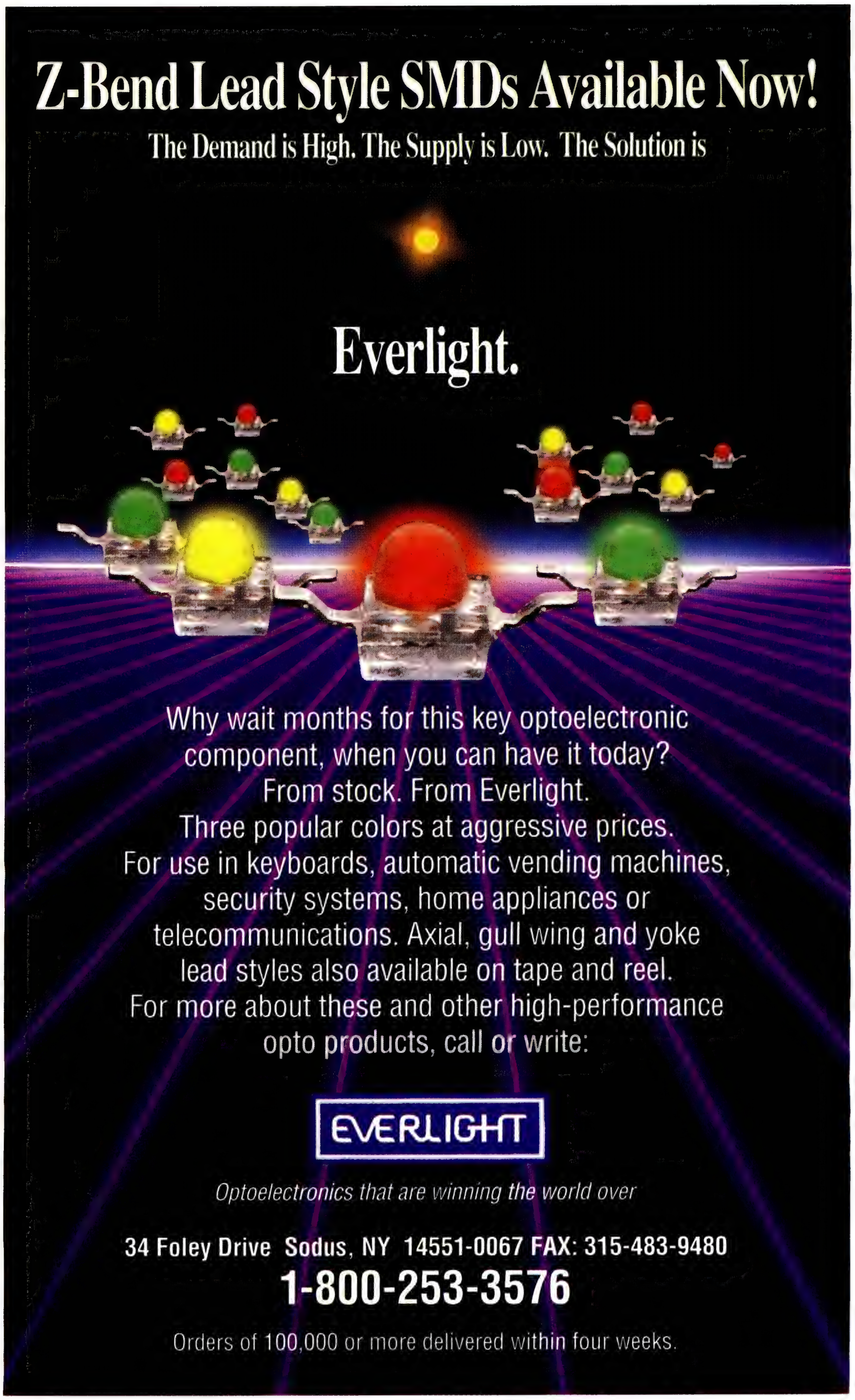
Included in the module is a standard flash memory chip and a custom logic chip, which provides the serial I/O control to the host system, and all the housekeeping to make the memory more intelligent. Thus, the module has two operating modes—at reset it can function just like a standard flash memory using the lower 32 pins on the package, or when sent a serial signal on one of new pins, the serial interface wakes up and the module serves as an intelligent serial device. When the serial port activates, the parallel bus interface to host system is disabled to ensure the flash memory does not receive conflicting requests. After the serial transfers, the serial port goes back to sleep and the parallel host interface is reactivated.

Each smart flash ROM (SFROM) is shipped with a unique and security-protected identifier code in the flash memory. The code acts as a target ID when one or more SFROMs are connected to the host in a serial loop. A simple download/upload program from Eurom can run on a PC and provide a simple serial data stream using a pin on the parallel port. The self-clocked serial data stream is decoded by the logic in the SFROM, which will either pass it through if the target ID doesn't match, or accept the data and update the memory if the ID matches.

The SFROM operates from 5 V and comes in standard DIP or surface-mount packages. In sample quantities, it sells for $30 each; in lots of 10,000, the price drops to $26. Samples are available now.

Eurom Ltd., 556 Mowry Ave., Ste. 103, Fremont, CA 94536; Danny Gur, (510) 505-9083. **CIRCLE 690**

■ *DAVE BURSKY*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FIELD-RECONFIGURABLE FPGA DELIVERS RECORD 16K USEABLE GATES

DAVE BURSKY

Although it's a fleeting number, the approximate 16,000 usable gates offered by the EPF81500 field-programmable gate array set the latest record for FPGA complexity. The SRAM-based monolithic circuit is the largest member of Altera's Flex family of FPGAs. As part of the high gate count, the chip also contains 1500 flip-flops and 208 available user input/output lines. To keep the chip operating with a minimum of noise, designers also added an abundant number of power and ground pins, which bring the total package pin count to 280 or 304 pins (package dependent, PGA or QFP, respectively).

The SRAM-based cells allow designers to not only download the configuration pattern when the system first starts up or is reset, but also allows them to modify the configuration at any time by resetting the FPGA and loading in a new pattern. Furthermore, once systems are fielded, software updates can be downloaded, thus eliminating costly service calls. In addition, the Flex family characteristics are carried forward in the EPF81500—very predictable timing, a register-intensive architecture, a low standby power, and in-circuit reconfigurability.

The 1500 available flop-flops are divided between the array and the I/O pads—1296 flip-flops are available in the core of the array, while 204 are embedded in the I/O pads. The remaining four, of the 208 I/O pads, are dedicated as input-only pins. Within the array, the logic cells are arranged in blocks of eight logic elements and the 162 blocks are distributed throughout the core.

Each logic element contains both combinatorial and sequential logic, with four-input look-up tables in each combinatorial element capable of implementing any function of four variables in just 5 ns. Sequential elements are configurable as any of several flip-flop types and include synchronous and asynchronous Load, Clear, and Preset inputs. Moreover, the flip-flops can be bypassed when the logic element is used in its combinatorial mode. The logic array block includes special cascade-connect features that allow designers to implement high-speed, wide-input functions, and carry chains for fast adders and counters.

Each block has three types of routing resources available to it—local routing (FastTracks) within the logic block that have 1 ns propagation delays, column FastTracks that have 3-ns delays, and row FastTracks that have 5-ns propagation delays. Thus, just 9-ns of cross-chip delay is encountered by any signal that makes it past the I/O pads. Using the local FastTracks and the cascade capability, eight-input functions have a delay of 6 ns, twelve-input functions require 7 ns, and sixteen-input functions need 8 ns. Such numbers are significantly faster than the delays encountered in other array families that implement functions with wide inputs.

The short cross-chip delays and the short logic-element delays allows functions such as counters, adders, data-paths, and others to operate at speeds close to 80 MHz.

Because the array is based on static RAM configuration cells, the standby power of the chip is very low—just 0.5 mA—while the active current when running from a 5-V supply is about 80 mA. Depending on the circuit configuration, the power consumption actually spans a wide range.

Supporting the design of the complex circuits, Altera has enhanced its MAX+Plus II family of development tools to handle the higher capacity of the new array. The tools will include a new compiler and a new fitter that will improve the gate-usage efficiency of the software, thus putting more of the system logic on one chip. The tools will also offer a more gate-array-like design-entry methodology, because this large FPGA gives designers densities that closely match popular gate-array complexities.

Samples of the array are now available in the 304-lead quad-sided flat package. In lots of 100 units the chip sells for $495 each. The "power" PQPF includes an embedded metal slug to remove heat.

Altera Corp., 2610 Orchard Parkway, San Jose, CA 95134-2020; Cliff Tong, (408) 894-7000. **CIRCLE 691**

CLOCK DISTRIBUTION IC SYNCS MULTIPLE LINES

With the ability to generate clock signals with frequencies from 10 to 125 MHz, the DA400 clock distribution circuit combines programmable timing generations, adjustable phase delays, and eight buffered outputs. Targeted for systems based on the Intel Pentium or IBM/Motorola PowerPC processors, the chip is fabricated in AT&T's digital bipolar BEST-1 process and comes in either a 44-lead ceramic package or a plastic leaded chip carrier with built-in heat spreader.

Each of the DA400's eight TTL-compatible outputs has programmable phase-delay circuitry, which allows the delays to be set to as little as 250 ps. To achieve tight skew tolerances, the chip employs an internal feedback scheme that synchronizes the input and output clocks, thus trimming the delay to near zero. That reduces the chip-to-chip skew in applications that would require multiple distribution chips. In addition, clock-edge synchronization is independent of temperature, thus easing system design.

Samples are immediately available. In quantities of 5000 units, the chip sells for $25.50 each.

***AT&T Microelectronics,** Dept. AL-500404200, 555 Union Blvd., Allentown, PA 18103; (800) 372-2447.* **CIRCLE 692**

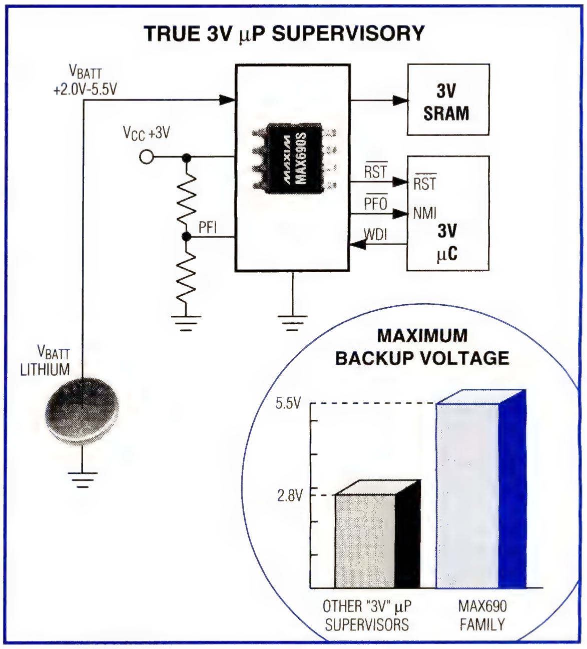
■ *DAVE BURSKY*

+3V µP SUPERVISORS SOLVE TOUGH BATTERY BACKUP PROBLEM

Backup Battery Voltage Can Be Greater Than A Valid +3V V_{CC} Without Causing False Switchovers

This family of 3V µP supervisors has been specifically designed for +3V systems. **These devices are not respecified +5V ICs.** They offer true battery-backup switchover, which is difficult to achieve at 3V. Choosing the higher of the backup battery or main supply—as 5V µP supervisors do—would lead to erroneous backup switchovers, since the backup battery is typically greater (3V to 3.6V) than the main power supply (2.7V to 3.6V) during normal operating conditions. The MAX690R/S/T, MAX704R/S/T*, and MAX804-MAX806R/S/T* avoid this problem by switching over to the backup battery only when the main supply has fallen below 2.4V.

- **RESET and $\overline{\text{RESET}}$ Outputs**
- **3 RESET Trip Thresholds:**
  3.0V-3.15V — "T" Suffix
  2.85V-3.00V — "S" Suffix
  2.55V-2.70V — "R" Suffix
- **Battery-Backup Switchover**
- **1.6 seconds Watchdog Timer**
- **40µA I_{SUPPLY} (Operating Mode)**
- **1µA I_{SUPPLY} (Backup Mode)**
- **Power-Fail Warning**
- **Manual-Reset Input**
- **Guaranteed $\overline{\text{RESET}}$ Assertion to V_{CC} = 1V**
- **8-pin DIP and SO Packages**



The MAX690 3V µP supervisor family allows the backup battery to be greater than V_{CC} (unlike other µP supervisors which limit it to 2.8V), thus making it possible to use a 3V lithium backup in a 3V system.

µP SUPERVISORY ANALOG DESIGN GUIDE 5

Data Sheets • Applications Notes • Free Samples

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GRAPHICS ACCELERATOR OPTIMIZED FOR 32-BIT PCI BUS

By optimizing the design of a graphics accelerator for use on the 32-bit peripheral-component interconnect (PCI) bus, Digital Equipment Corp. was able to craft the fastest graphics accelerator chip for moderately priced desktop systems. The company's DECchip 21030 graphics accelerator is the first in a family of graphics chips that will be developed and marketed jointly with Brooktree. Included on the chip is support for 2D graphics in both Microsoft Windows NT and Windows environments, as well as 3D graphics using OpenGL.

With the ability to draw as many as 2.3 million 10-pixel random-oriented lines per second, the chip delivers close to double the drawing speed of just about all current "best-of-breed" graphics accelerators used in PCs. In addition, for 3D images, the chip can draw 63,000 Gouraud-shaded Z-buffered triangle-shaped polygons per second. Such performance is comparable to low-end and mid-range workstations.

For common operations, such as fills, the chip can transfer data at 640 Mb pixels/s; for solid fills and brushed fills for Windows, the chip can deliver those high transfer rates even for true-color pixels, thanks to proprietary frame-buffer addressing schemes that can move the data very quickly. The accelerator can support 24-plane 1600-by-1280 pixel true-color graphics at the high end, and go down to VGA pass-through on the low end.

Furthermore, DEC has included some proprietary (patented) dithering technology, which will allow the chip to produce images with 16-bit/pixel quality, but starting with only 8 bits/pixel. The proprietary dithering scheme employs an ordered, multilevel approach that minimizes the hardware requirements, yet delivers a high-quality image.

On the chip, the dithering outputs are run through a simple color mapping look-up table to perform the color-space conversion—that avoids costly dematrixing and also allows infeasible RGB values to be intelligently mapped back to feasible space off-line, during the generation of the color-mapping lookup table.

Pixel depths of 8, 12, 24, or 32 bits can be handled, and users pay no performance penalty when transferring 24-bit pixels (true-color) rather then 8-bit pixels. In contrast, many current graphics accelerators must switch to a lower screen resolution if they transfer deeper pixels. An on-chip copy buffer, and high-speed double and triple buffering, allows the chip to easily handle real-time animation applications. A 64-bit interface between the controller and the frame buffer allows for high-speed data transfers and fast bit-block transfers.

The 240-lead PQFP-housed CMOS chip ties directly to a 32-bit Brooktree RAMDAC, and can directly control from 1 to 8 Mbytes of video RAM or DRAM-based frame-buffer memory without any glue logic. Futhermore, the 21030 supports linear addressing of up to 16 Mbytes, Z-buffering, VGA pass-through, and includes a 64-by-64-by-2 pixel hardware cursor. Drivers for the chip are being developed by both DEC and Brooktree, with DEC concentrating on the Windows NT and 3D drivers, and Brooktree concentrating on developing the DOS and Windows drivers.

When clocked at 38 MHz and powered by a 5-V supply, the 21030 consumes about 2.25 W, worst case. Samples of the chip are immediately available. In lots of 5000 units, the accelerator sells for $59.80 each. Brooktree will have samples next quarter. Two evaluation boards, complete with full design documentation, are also available from DEC. The first is an accelerator card with 2 Mbytes of RAM that lists for $850, and a true-color version with 8 Mbytes of RAM that lists for about $2100. Documentation includes schematics in ViewLogic format, thus enabling designers to easily modify the design.

***Digital Equipment Corp.**, 77 Reed Road, HLO2-3/M7, Hudson, MA 01749; (508) 568-5149.* **CIRCLE 693**

***Brooktree Corp.**9950 Barnes Canyon Road, San Diego, CA 92121; Allyn Pon, (619) 535-3464.* **CIRCLE 694**

■ *DAVE BURSKY*

SUBNOTEBOOK 486 LOGIC SUPPORT IN TWO CHIPS

Housed in a pair of 176-lead thin PQFPs, the QuadNote chip set includes all major system and peripheral blocks required for designers of subnotebook computers. The first of the two chips, the VL82C410, packs the CPU interface, DRAM controller, 486SL-style power management, a real-time clock, and VLSI's own multiplexed local bus (MLB) interface. Providing the peripheral interfaces, the other chip, the VL82C142, contains the 80C51-type keyboard controller, an extended capabilities parallel port, an infrared communications port based on a 16C550-type UART, an IDE disk controller, a real-time clock, and two pulse-width modulators for LCD panel contrast and brightness control or dc-to-dc conversion control.

The high integration creates a glueless interface to the 80486-class CPU and allows designers to also tie in the 100-lead ExCA-compatible PCMCIA controller on the MLB (also available from VLSI Technology). With the ability to run from either 3.3- or 5-V power supplies, the set supports CPUs that operate at external frequencies of up to 33 MHz. Samples of the QuadNote chip set are available now. In lots of 10,000 units, the chips sell for $30 and $21 apiece, respectively, for the VL82C410 and 142. The 82C146 PCMCIA chip goes for $8.50 each in similar quantities.

***VLSI Technology Inc.**, 8375 South River Parkway, Tempe, AZ 85284; Joe Barta, (602) 752-8574.* **CIRCLE 695**

■ *DAVE BURSKY*

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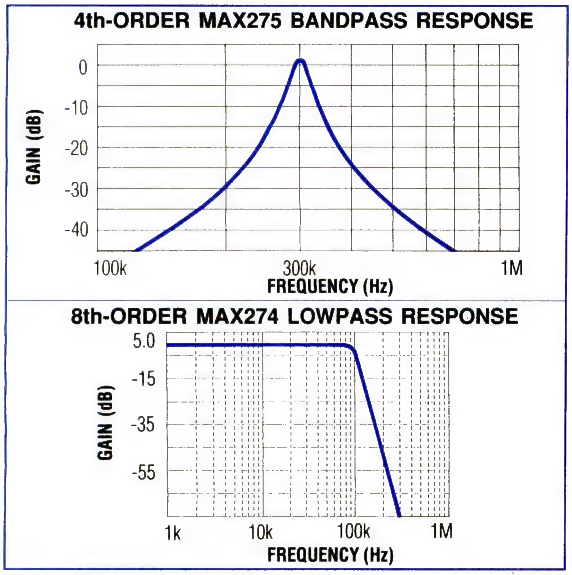

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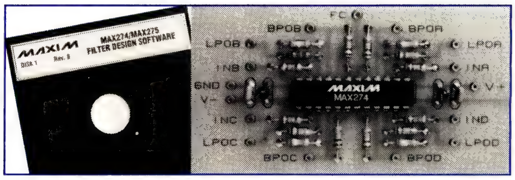

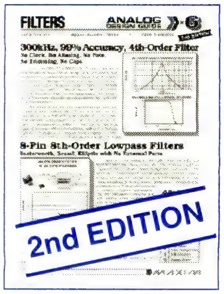
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DSP-BASED ACQUISITION UNIT OFFERS 16-BIT RESOLUTION

The DAQ-200 DSP-based data-acquisition system features a programmable sampling rate of up to 200 kHz, and a resolution of 16 bits. Enclosed in its own metal box with its own linear power supply, the unit virtually eliminates RFI and power-supply noise. The dual-channel system can be used in standalone or embedded DSP applications.

The system uses a combination of careful analog design, including optical isolation of analog and digital sections, and DSP techniques to achieve the full 16-bit performance from its analog-to-digital and digital-to-analog devices. Special analog parts and a circuit topology for low noise and distortion provide a usable dynamic range in excess of 110 dB. Total harmonic distortion plus noise is specified at less than –86 dB, and signal-to-noise ratio is greater than 88 dB. Each unit is characterized for THD+N and signal-to-noise ratio, with results supplied to purchasers.

Operators can use the system's DSP functions to perform 4:1 decimation of the input, and 1:8 interpolation of the output. By decreasing sampling rate in this manner, the DAQ-200's specifications are improved by about 6 dB.

The DAQ-200 is based on the Texas Instruments TMS320C31 33-MFLOPS DSP device, which allows it to perform functions that would otherwise require a separate DSP subsystem. With a digital I/O card in a PC as an interface, the DAQ-200 is supported by several Windows-based applications for general DSP design and data acquisition. These include Hyperception's Block Diagram, Momentum Data Systems' DSPWorks, Signalogic's DSPower, and MathWork's MATLAB.

The DAQ-200 costs $2495, with delivery within four weeks.

***Sonitech International Inc.**, 14 Mica Ln., Wellesley, MA 02181-1708; (617) 235-6824.* **CIRCLE 696**

■ *JOHN NOVELLINO*

THERMAL IMAGE SYSTEM USES PC PLUG-IN CARD

Engineers using thermal imaging to evaluate product reliability can now use a PC-based system that eliminates the need for redundant displays, processors, and disk drives. The PC-2000 comes with a system card that plugs into an 8- or 16-bit expansion slot on any IBM-compatible PC and connects via cable to an infrared (IR) camera. The camera scans the products under test and displays a thermal map on the PC's high-resolution VGA display. The system's menu-driven software offers easy storage, retrieval, and analysis of the image. Electronic zoom and temperature profiling are included. Images are stored in the tagged image file format (TIFF). A PC2000e version substitutes an external module that can be plugged into a laptop computer. The PC2000 is available within six weeks, and the PC2000e within eight weeks. Typical systems cost less than $10,000. JN

Compix Inc., P. O. Box 885, Tualatin, OR 97062-0885; (800) 926-6749 or (503) 639-8496. **CIRCLE 697**

UNIT PROGRAMS MEMORY CARDS AND DEVICES

The M4016 programmer handles standard PCMCIA memory cards and in-circuit programming of custom memory cards as well as standard programmable devices. The unit employs adapters to change between devices and cards, with a typical adapter containing four device or card sockets. Packages like PLCC and SOP are handled with small scrambler sockets. Adapters are available for 8- and 16-bit EPROMs, 8-Mbit EPROMs (42- and 48-pin devices), EEPROMs, flash EPROMs, the 8751 family of microcomputers, and PCMCIA cards. The programmer has a full-edit hexadecimal keyboard, a backlit LCD graphics display, and RS-232, Centronics parallel, and SCSI interfaces. Both DOS and Windows support is available. A typical M4016 system costs about $10,000. Delivery is from stock. JN

International Microsystems, 521 Valley Way, Milpitas, CA 95035; (408) 942-1001. **CIRCLE 698**

PC-BASED DMM FEATURES 5-1/2-DIGIT RESOLUTION

The SM2020 is a 5-1/2-digit digital multimeter built onto a single-slot PC plug-in board. The unit takes up to 200 readings per second and maintains 5-1/2-digit resolution to 60 readings per second. Functions include ac and dc volts in four ranges to 300 V, ac and dc current in three ranges to 30 mA, and two-wire and four-wire resistance in six ranges to 30 MΩ. True RMS ac measurements are made from 20 Hz to 100 kHz. Software support includes Windows dynamic link libraries, DOS libraries for VisualC++ and QuickC, DOS and Visual Basic virtual front panels with sources, and one-step setup. Additional drivers are available for ATEasy, LabWindows, and LabView. The SM2020 costs $995. A counter-trigger option is $195. Delivery is in four weeks. JN

Signametics Corp., 3525 N.E. 94th St., Seattle, WA 98115; (206) 524-4074. **CIRCLE 699**

2.4-GHZ COUNTER BOASTS 0.5-ppm TIMEBASE

The Model 1856A microwave multifunction counter has a 5-Hz to 2.4-GHz bandwidth, with a 50-mV sensitivity at 2.4 GHz. The unit features a temperature-compensated crystal oscillator timebase with 0.5-ppm stability from 18 to 28°C, and 1-ppm stability from 0 to 50°C. For accurate measurements at low frequencies, the counter makes period measurements from 0.28 μs to 0.2 s. This function facilitates measurement of tone-encoding frequencies used in many communication systems. In totalize mode, the instrument counts pulses from 5 Hz to 10 MHz up to 99,999,999. Reset and hold can be performed using a front-panel switch or a remote start-stop input. The Model 1856A costs $499 and is available from stock. JN

B+K Precision, 6470 W. Cortland St., Chicago, IL 60635; (312) 899-1448. **CIRCLE 700**

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3µA Comparator + Voltage Reference + Adjustable Hysteresis in 8-pin SO

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- **On-Board 1.2V ±1% Reference**
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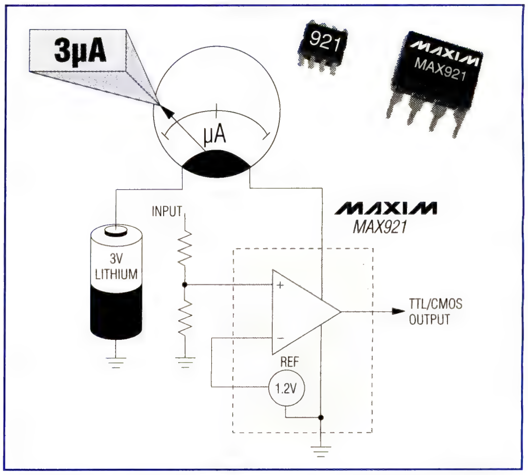
  - **Input Range Includes GND**
  - **Dual Supply: ±1.25V to ±5.5V**
- **Adjustable Hysteresis**
  - **No Effect on High-Z Inputs**
  - **Independent of Supply Voltage**
- **TTL/CMOS Compatible Outputs**
  - **No Pull-ups Required**
- **Output Sources 40mA**
  - **12Ω High Side Load Switch**



Operating current for the MAX921 comparator is equivalent to battery leakage current.

Ideal for battery-powered applications, the MAX921 draws less than 3µA from a single lithium cell, with only 12µs prop. delay. The IC includes a 1.2V ±1% reference, and its TTL/CMOS-compatible output requires no pull-up resistor. One pin lets you add hysteresis without affecting the high-impedance inputs. Dual and quad versions are also available.

Choose the Lowest Power Comparators for Battery-Powered Systems

Device		Total Supply Current (µA Max, 25°C)	1.2V Reference Over Temp (% Max)	Adjustable Hysteresis	Package	Price†
MAX921	Single + Reference	3	±1	✓	8-DIP/SO	$1.50
MAX922	Dual	3	N/A		8-DIP/SO	$1.50
MAX923	Dual + Reference	4	±1	✓	8-DIP/SO	$1.95
MAX924	Quad + Reference	7	±1		16-DIP/SO	$2.25

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MODULAR BOARDS AND CHASSIS FILL OUT EMBEDDED-SYSTEM LINE

The Embedded Modular Computer (EMC) line of system components has grown with the addition of five cards and two chassis. The modules include the EXM-19, a 24-line optoisolated digital I/O module ($179); the EXM-23, an LCD controller for monochrome and color displays ($247); the EXM-24, an intelligent eight-port serial RS-232 communications module ($825); the EXM-28, an Arcnet networking module ($208); and the EXM-29, a Fastcomm/422-compatible dual-port RS-422/485 serial communications module ($200). The list of EXM modules now stands at greater than 20. All the modules are software compatible with the PC/AT bus.

The EMC-CH10D chassis can hold up to 10 EXM cards and connects to a floppy-disk module and power supply for easy integration into OEM automation equipment. It sells for $213. The EMC-CH6AT holds six cards and connects to a power supply and a standard PC/AT slot. The chassis and 50-W power supply sell for $950. The ruggedized chassis measure 4.14 by 5 in. All prices, for both the cards and chassis, are for quantities of 50 or more.

***RadiSys Corp.,** 15025 S.W. Koll Pkwy., Beaverton, OR 97006; (503) 646-1800.* **CIRCLE 701**

■ *RICHARD NASS*

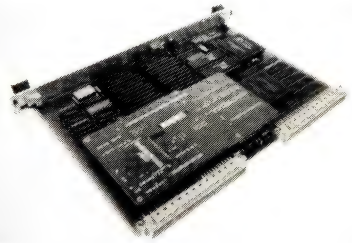
VME SBC HOLDS C40 DSP

Built with the Texas Instruments TMS320C40 floating-point digital signal processor, the 4284 forms the processing element of a complete VMEbus subsystem. The single-board computer holds 16 Mbytes of DRAM, 4 Mbytes of SRAM, 32 kbytes of EPROM, and ten front-panel communication ports. A MIX mezzanine-bus interface, which can accept three modules, offers further expansion. As a result, a system can be configured, for example, with 32 channels of 100-kHz analog-to-digital conversion with up to 450 MFLOPS of total processing power in a 3.2-in. VME card cage. The 32-bit, 20-Mbyte/s mezzanine interface is mapped directly to the DSP's local bus and includes full interrupt handling. An integrated software development environment supplies all the tools needed to develop real-time applications. List prices for the 4284 DSP-based VMEbus SBC start at $6495. Large-quantity discounts are available. RN

Pentek Inc., 55 Walnut St., Norwood, NJ 07648; (201) 767-7100. **CIRCLE 702**

GDC SUITS RUGGED, MILITARY ENVIRONMENTS

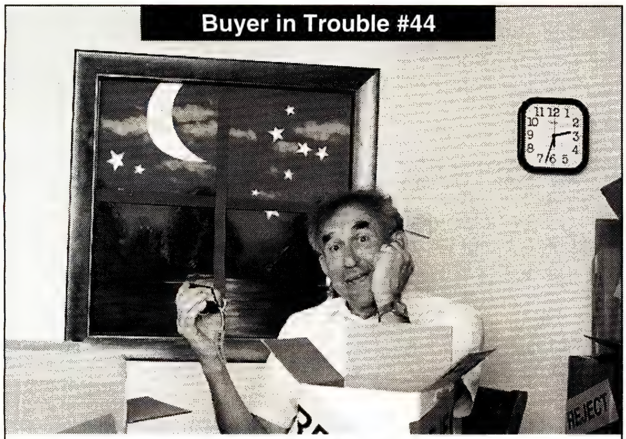
The SVME/DMV-770 is a graphics display controller (GDC) that's designed for commercial, rugged, and military VME applications. The display engine, which runs high-resolution raster graphics, supports the overlay of color symbology and graphics on monochrome or color sensor inputs.



The board can drive either CRT or flat-panel displays, with an option for a dual-display drive. The on-board graphics is handled by a TMS34020 processor. Various software graphics command sets are available, including an optimized real-time graphics system and standard X-Windows. Different versions are available, depending on the intended operating environment. RN

DY 4 Systems Ltd., 1475 S. Bascom Ave., Suite 202, Campbell, CA 95008; (408) 377-9822. **CIRCLE 703**

Buyer in Trouble #44



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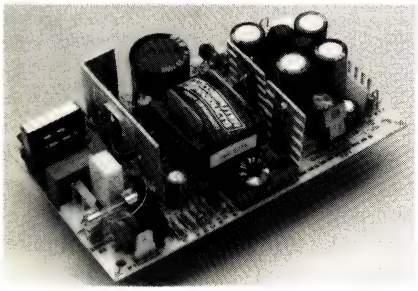
READER SERVICE 123

LOW-COST SWITCHERS PROVIDE 25 OR 40 W

Targeting price-sensitive applications, the NAL family of 25- and 40-W switching supplies comes in dual- and triple-output versions, features a 90-to-264-V ac universal input, and occupies a 5-by-3-by-1.2-in. space.



Outputs offer a total regulation band of ±3% on the main output and ±5% on the auxiliary output(s). Ripple and noise are specified at 1% pk-pk on all outputs. All required safety approvals are included and the supplies meet FCC Level B and VDE Level A emissions standards. Typical prices are $18 for the NAL25 and $19 for the NAL40 in OEM lots. DM

Computer Products/Power Conversion America, 7 Elkins St., South Boston, MA 02127; (617) 464-6656. **CIRCLE 704**

SOFT-START THYRISTOR BRIDGE CUTS EMI

A family of modules combines a full-wave bridge rated at 36 A and 1200-to-1600 V with an integrated 36-A soft-start thyristor. The thyristor reduces a cause of electromagnetic interference by bringing the dc voltage up slowly to avoid in-rush currents, which cannot be tolerated in computer power supplies. The bridges are designed to operate off the 380- to 575-V ac lines and provide the dc voltage for switched-mode and six-step power supplies. This hybrid module consists of a flat plastic package, with a direct copper bonded ceramic base plate, and printed-circuit-board solderable leads. The modules' isolated construction permits designers to mount them directly to a heat sink with screws and washers. In lots of 100, prices start at $20.66 each. FG

IXYS Corp., 3540 Basset St., Santa Clara, CA 95054; Ralph Locher, (408) 496-06780. **CIRCLE 706**

500-V IGBTS SWITCH AT UP TO 100 KHZ

Designed for uses ranging from large switchers and UPSs to lamp ballasts, a new family of six "Ultra Fast" 500-V IGBTs switch efficiently at frequencies to 100 kHz. Current ratings range from 14 to 59 A. The IGBTs are also available paired with "Hexfred" fast-recovery diodes, in five new "Co-Packs" for totem-pole half-bridge, full-bridge, and three-phase-bridge applications. Both discrete IGBTs and the Co-Packs come in TO-220 and -257 packages. The company added a new speed benchmark, the half-current frequency, to its IGBT data sheets. This is the frequency at which the device can switch half the maximum rated continuous dc current. In lots of 1000, prices are $1.50 to $10 each. FG

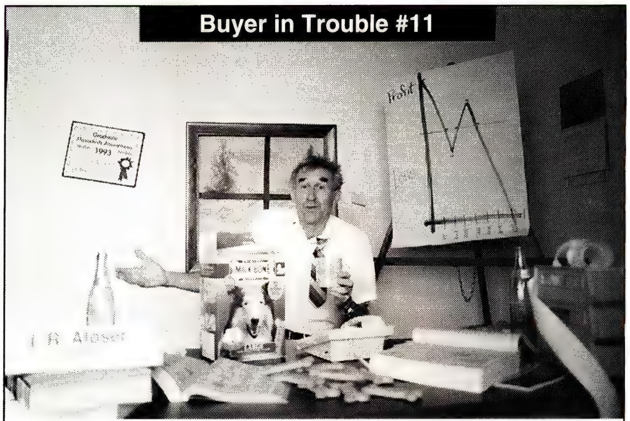
International Rectifier Corp., 233 Kansas St., El Segundo, CA 90245; Chris Ambarian, (310) 607-8815. **CIRCLE 707**

FIELD RINGS RAISE FETS BLOCKING VOLTAGE

By adding a patented array of multiple field-termination rings to all power MOSFETS rated to block 400 or more volts, Motorola has substantially enhanced their voltage blocking capability. These rings, around the edge of the die, protect against surface charges that commonly occur at the chip's junction termination when high voltage is applied. New 1000-V n-channel FETs with these rings include: the 10-A MTY10N100, which has an on resistance of 1.3 Ω, comes in a TO-264 package and costs $21 each in lots of 1 to 999; the 6-A MTW6N100E, which has an on resistance of 1.5 Ω, comes in a TO-247 package, and costs $12.50 each in lots of 1-999; and the 3-A MTB3N100E, which has a 4 Ω on resistance, comes in a D^2 PAK, and costs $5 each in lots of 1-999. FG

Motorola Inc., MD Z-310, 5005 E. McDowell Rd, Phoenix, AZ 52073; Trudy Mystrom, (602) 244-3576. **CIRCLE 705**

Buyer in Trouble #11



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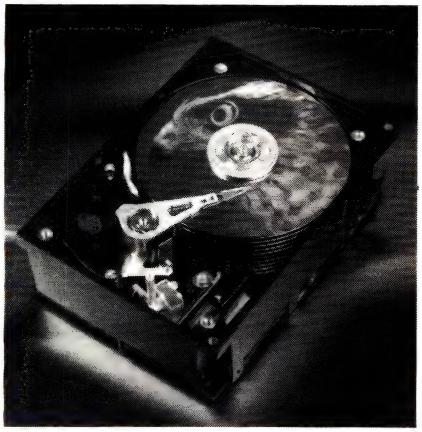
3.5-IN. DRIVE STORES 4.3 GBYTES



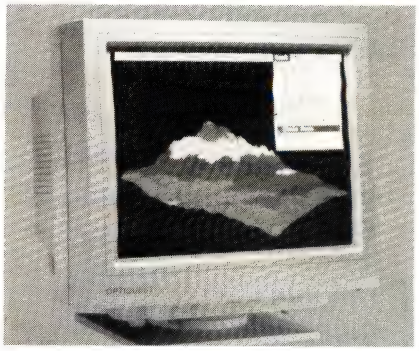
The Hawk 4 3.5-in. disk drive stores 4.3 Gbytes on its 10 platters. Suited for file-server, disk-array, and workstation applications, the drive features an average latency of 5.56 ms, an average read seek time of 9 ms, and a 512-kbyte multisegmented adaptive cache memory. These specifications result from the drive's 5400 rpm. Data is transferred externally at a rate of 20 Mbytes/s, while internal transfers take place at 64 Mbits/s. The Hawk 4 is based on either fast SCSI-2 or fast and wide SCSI-2, in single-ended or differential configurations. A Single-Connector Attachment (SCA) interface is also available which is suited for disk-array and server applications because it eliminates the need for multiple cables and drive-configuration settings. The mean-time between failure is rated at 800,000 hours. The drive costs $2250. Evaluations units are available now, with production starting in the second quarter. RN

Seagate Technology Inc., 920 Disc Drive, Scotts Valley, CA 95066; (408) 438-6550. **CIRCLE 708**

17-IN. MONITOR ADDS ENERGY STAR COMPLIANCE

Energy Star compliance has been added to the 4000DC color monitor, which also incorporates on-screen programming for precise control of monitor adjustments. When not in use, the display powers down to less than 5 W. The 17-in. non-interlaced display is built with an anti-reflection, anti-glare, flat-square CRT. An Invar shadow mask increases image crispness and brightness by 20% over traditional CRTs. The 4000DC offers a dot pitch of 0.27 mm, a maximum resolution of 1280 by 1024 pixels, and a maximum refresh rate of 76 Hz. The low-power display sells for $899. RN

Optiquest Inc., 20490 East Business Pkwy., Walnut, CA 91789; (909) 468-3750. **CIRCLE 709**



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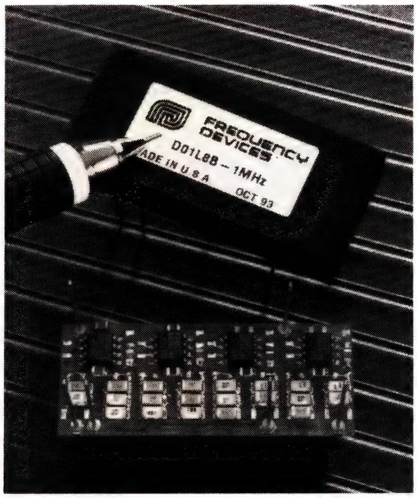
Circle 170 For Literature

DIP ACTIVE FILTERS CORNER AT UP TO 1 MHZ

In the past, it's been difficult, if not impossible, to find a precise, high-order active filter that offered high corner frequencies. Instead, the designer would be forced to turn to passive filtering for such applications. But with Frequency Devices's introduction of the D01 Series of linear active filters, corner frequencies of up to 1 MHz are now available in a plug-in, ready-to-use 32-pin DIP that minimizes board space.

Passive filters contain inductors that introduce signal non-linearity and distortion. In addition, these inductors often must be shielded from the rest of the filter and from other circuit components. The internal loading in passive filters also contributes to insertion loss, and their limited attenuation floors of –40 to –60 dB are insufficient for high-precision data acquisition.



Active filters avoid use of inductors and provide total harmonic distortion to below –80 dB at 1 kHz with better than 80 dB of attenuation. They also provide monotonic roll-off in the stop band, resulting in superior filtered-signal integrity. Not only that, active filters offer high input impedance and low output impedance for effective isolation from other components.

The D01 filters use surface-mounted components and conform to classic 4-, 6-, and 8-pole Butterworth and Bessel transfer functions in a 1.8-by-0.8-by-0.3-in. package. Each filter comes factory tuned to a user-specified corner frequency from 50 kHz to 1 MHz. The plug-in filters are factory tuned and require no external clocks or adjustments. Applications include high-end data acquisition, magnetic imaging, data transmission, communications, and video. Prices start at $104 for a single 4-pole filter and drop to $74 in lots of 1000 or more. Delivery is in three to four weeks.

Frequency Devices Inc., *25 Locust St., Haverhill, MA 01830; Greg Anderson, (508) 374-0761.* **CIRCLE 710**

■ *DAVID MALINIAK*

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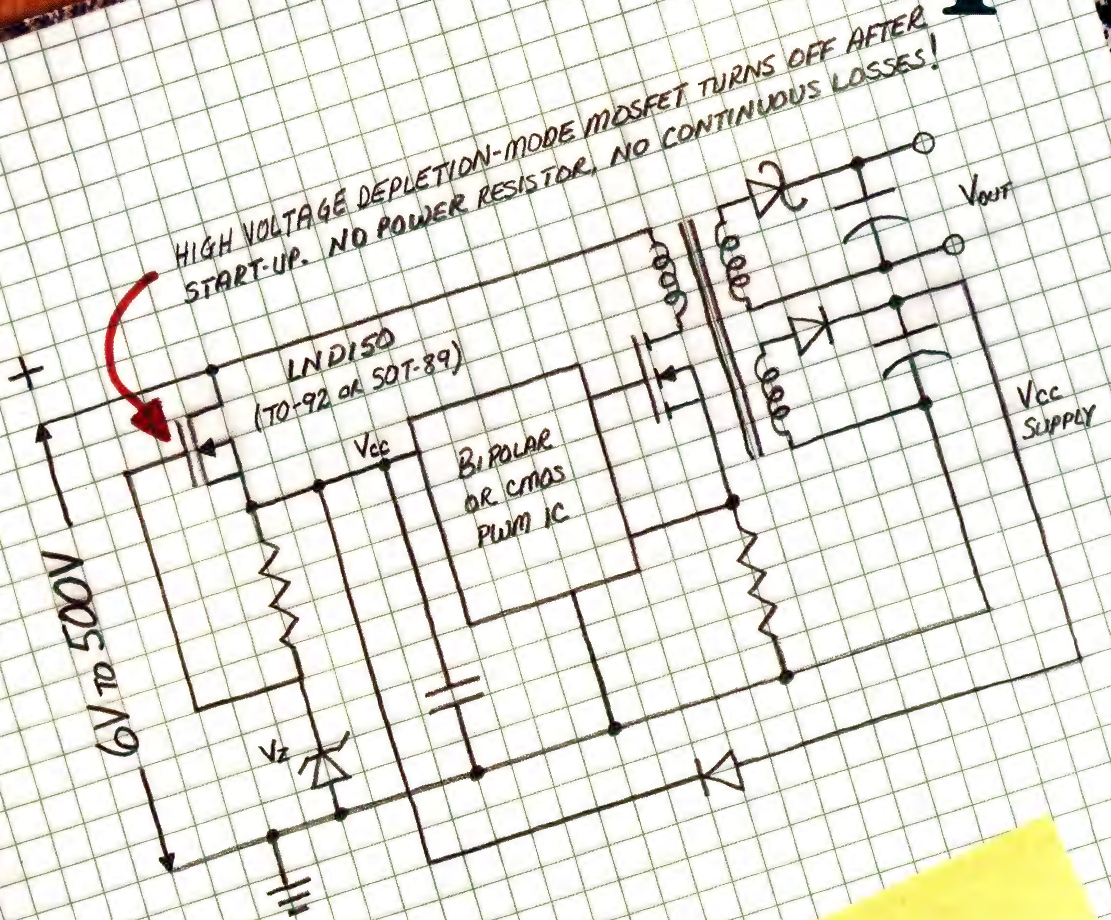
High Voltage SMPS Start-Up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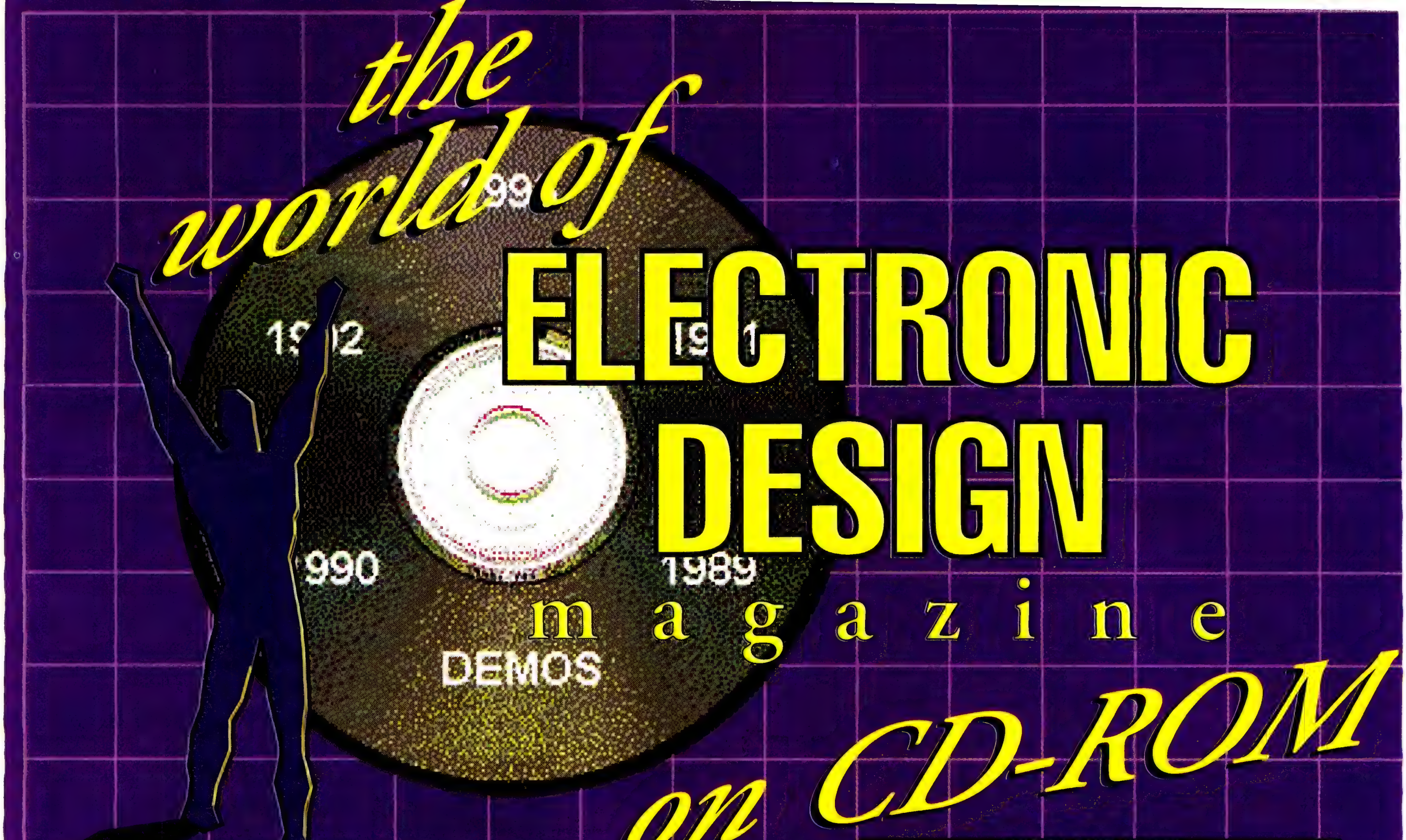

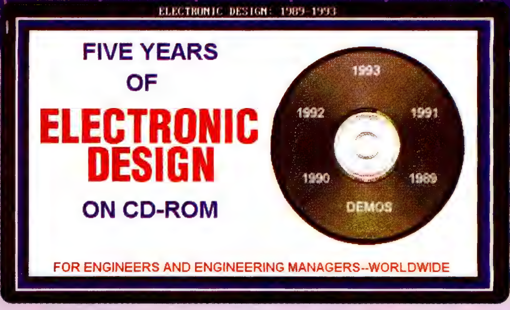
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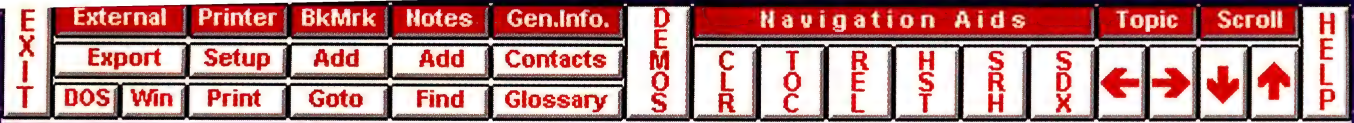
CONTENTS: MAY 13, 1993 VOL. 41, NO. 10

TESTER TAKES AIM AT MULTICHIP MODULES

THE SYSTEM COMBINES THE PERFORMANCE OF AN IC TESTER WITH THE FUNCTIONALITY OF A BOARD TESTER

JOHN NOVELLINO

Hypertext links exist between volumes, issues, articles, photos, and glossaries. Links also exist between past and subsequent related topics - makes getting the most current information simple!



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The EXIT button quits the application, and takes you right on out into the cold, cruel, computer world. If you want to leave the Electronic Design Magazine, and still have easy access without re-launching, use the **DOS** and **Win** buttons. These are located under **External** *(see below).*

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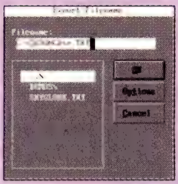

The **Export** button will export any or all of an article based on your selection.

DOS & Win - **DOS** brings you to the DOS prompt screen and **Win** takes you into Windows™ without quitting the application. Return to Electronic Design Magazine, where you left off, without re-launching.

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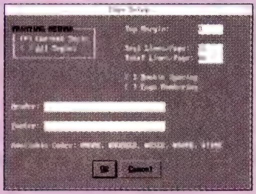
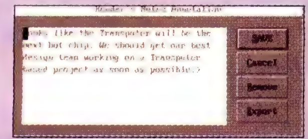


Setup & Print - Articles, editorials, glossaries, table of contents, illustrations, and photos (if your printer is capable).

Bookmarks and Notes - *Leaving your mark*

BkMrk - Bookmarks flag topics for future reference, just like using a bookmark in a real magazine. You mark a spot, and the bookmark is stored even if you quit. **GOTO** brings you back to your bookmarks. Deleting them is just as simple.

Notes - Add and find your own notations. Notes stay until you delete them, even after you quit.


Looks like the Transputer will be the next hot chip. We should get our best design team working on a Transputer based project as soon as possible.>

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Glossary - Full article glossaries, provided by the Editors of Electronic Design magazine. The CD also comes with **WORD LINK**, which allows you to click on any word within the article and if it's in the glossary, the definition pops up. When you're done, a simple click and it's gone.

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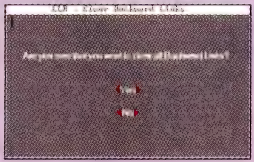

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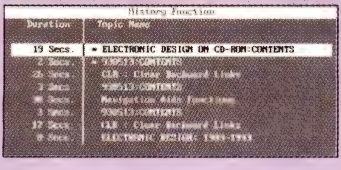
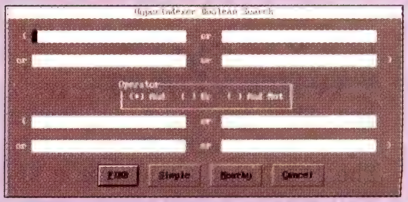
TOC - ***Table of Contents*** - Takes you directly to the Volume Table of Contents (the whole year) with special links provided to Issue T.O.C.

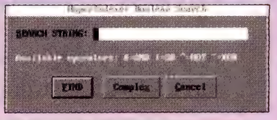
REL - ***Show-Related Articles*** - Calls up a list of, and lets you move to, related topics.

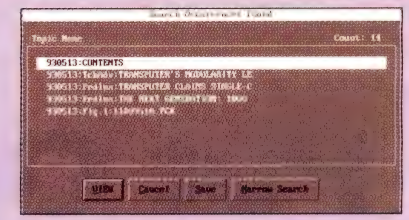
HST - ***Show-Related History*** - Shows each topic visited during your current session and how long you were there, and then lets you return to previous topics.



13 Secs. * ELECTRONIC DESIGN ON CD-ROM:CONTENTS







930513:CONTENTS

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SDX - ***Subject Index*** - A hierarchical list of key subject areas compiled by the Editors of Electronic Design. The index also allows direct access to related topics.

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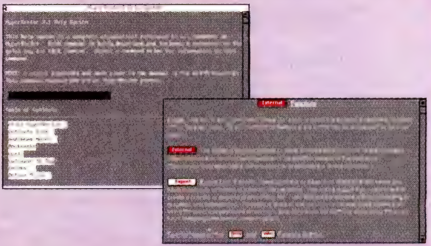

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The AD420, a 16-bit d-a converter, can drive 4- to 20-mA current loops. The DAC also allows for a single-chip interface between a microprocessor and the standard current loop. The converter is powered by one 12- to 36-V supply, over a temperature range of –40° C to 85° C, with an output of 0 to 5 V, 0 to 10 V, or ±10 V. Features include an asynchronous clear pin, 0 to 24 mA over-range capability, and provisions for an external output transistor. Peripheral circuitry allows for the detection of loop faults and an on-chip precision voltage reference. The AD420 offers a serial port interface, which is compatible with the SPI and MicroWire processors. It comes in a 24-pin SOIC or DIP and costs $100 each, in lots of 100. CA

Analog Devices, Inc. 181 Ballardvale St., Wilmington, MA 01887, (617) 937-1428. **CIRCLE 711**

VIDEO SWITCH FEATURES 8-Ω ON RESISTANCE

The DG643 dual single-pole, double-throw analog switch provides a –3-dB bandwidth of 500 MHz. This bandwidth reduces group delay and preserves rise and fall times when switching digital signals. The ac performance combines with a typical on resistance of just 8 Ω and a low on-state capacitance of 10 pF. In a 16-pin DIP, the DG643 costs $1.80 each, in lots of 1000. For 16 cents more, it comes in a 16-pin SI-16. FG

Siliconix, P.O. Box 54951, Santa Clara, CA 95056-0951; (800) 554-5565, ext. 99. **CIRCLE 712**

PRECISION OP AMP OFFERS LOW NOISE, CHEAP PACKAGE

The OPA124 is a precision monolithic FET operational amplifier that offers versatility, performance, small size, and low price. Made with Burr-Brown's Difet (electrical isolation) fabrication process, it has a maximum low input-bias current of 1 pA, maintained over a wide-input common-mode voltage range with unique cascade circuitry. This cascode design allows for high-precision input specifications and reduces susceptibility to flicker noise. Key features include low voltage noise of 6 nV/Hz at a frequency of 10 Hz, a high open-loop voltage gain of 120 dB (minimum); 125 dB (typical), and a high common-mode rejection of 90 dB (minimum); and 100 dB (typical). In addition, a low offset of 250 τV (maximum) and drift of 2 τV°C, is achieved through laser trimming of thin-film resistors. The OPA124 comes in an 8-pin package with either plastic DIP or SOIC formats. The amplifier is available from stock and in lots of 1000 costs $3.12 each. CA

Burr-Brown Corp., P.O. Box 11400, Tucson, AZ, 85734; Mary Douglass, (602) 746-1111. **CIRCLE 713**

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Digital Equipment Corp.

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Mr. Mario Mazzola, Vice President, Cisco Systems

System Implications of ATM
Dr. Daniel Abensour, ATM Systems Manager, IBM Corp.

Network Component Directions
Charles Carinalli, Senior V.P and Chief Technical Officer, National Semiconductor Corp.

Tuesday, April 5: Three full-day Tutorials

Tutorial 1: Asynchronous Transfer Mode
Tutorial 2: High-Speed Interconnections (100-Mbit Ethernet, Fibre Channel, Scalable Coherent Interfaces, P1394, QuickRing, etc.)
Tutorial 3: Internetworking and Network Management Approaches

Wednesday, Thursday, April 6, 7:

Technical Papers, Panel Sessions and Exhibits

The conference is divided into three parallel session tracks that will present technical papers and panels highlighting design approaches and issues in various themes:

* *Implementing ATM, Fibre Channel, Sonet, SCI, 100base-VG, CDDI/FDDI, and other high-speed WAN, LAN and point-to-point networks and network adapters.*
* *Network management and diagnostic approaches.*
* *Design approaches for high-performance internetworking products (bridges, routers, etc.).*
* *Wireless network interfaces.*

roduct Exhibits: Noon-2:00 pm, April 6 & 7

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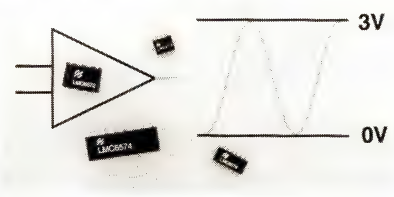
SINGLE-SUPPLY CMOS OP AMPS GUARANTEE OPERATION AT 2.7 V



Unknown to most digital IC and system designers, analog ICs which can operate with less than 5 V between its supply rails—such as the late Bob Widler's LM10 op amp—are not new. But due to the on-going demand for such devices, National Semiconductor has a new dual and a quad CMOS op amp with all its specifications given (most guaranteed) while running off a 2.7-V rail. The LMC6572 and LM6574 guarantee rail-to-rail output swings, within 20 mV of either rail, while driving 100 kΩ connected between the output and half the supply voltage. Though maximum bias current over temperature is a mere 10 pA, at 25 °C it's typically an unmeasurable 0.02 pA. Quiescent current at 2.7 V is a maximum of just 60 μA per op amp, but they can typically source 6 mA and sink 4 mA. However, these are real op amps. Open-loop gain typically runs better than 114 dB driving 100 kΩ.

With their low quiescent current and supply voltage, these op amps are not speed demons. Maximum slew rate for a 1-V input step, while connected as a follower, runs 30 V/ms, and typical unity-gain bandwidth a mere 220 kHz. The dual LMC6572 comes in 8-pin DIPs and SOICs in the standard pin out; the quad LMC6574 comes in similar 14-pin packages. In lots of 1000, pricing for the former starts at $1.35 each, and for the latter at $1.85 each.

National Semiconductor, P.O. Box 58090, M/S 16.300, Santa Clara, CA 95052-8090; Angelo Pietroforte, (408) 721-5856.
CIRCLE 714

■ *FRANK GOODENOUGH*

ANALOG SWITCHES BOAST 883B COMPLIANCE

Three precision analog switches—the DG417, DG418, and DG419—offer low leakage, fast switching, low resistance, and comply with MIL-STD-883, Class B, Rev. D. The switches operate from a 15-V power supply, drawing only 1 μA of supply current at 25°C, with a maximum leakage of 250 pA at 25°C. Features include a maximum turn-on time of 175 ns, and a maximum turn-off time of 145 ns. The switches have a maximum on resistance of 35 Ω. The DG417 is a SPST normally open switch; the DG418 is a SPST normally closed switch; and the DG419 is a SPDT NO/NC switch. The switches come in a 8-lead CERDIP package. In lots of 100, the DG417/DG418 cost $8.16 each, and the DG419 costs $8.98 each. CA

Maxim Integrated Products, 120 San Gabriel Dr., Sunnyvale, CA, 94086, (408) 737-7600, ext. 6087. CIRCLE 715

SWITCH-CAPACITOR FILTERS HANDLE 150 KHZ

The SC60 and the SC64 switched-capacitor filters provide pin compatibility with the LTC1060/MF10 and the LTC1064, respectively. The former represents a quad second-order, universal switched-capacitor building block, which handles center frequencies to 150 kHz. The latter is similar but it is a dual, handling center frequencies to 140 kHz. Both use clocks to 7 MHz. The center frequency, gain, and Q of each section are controlled by the clock frequency, and three to five external resistors. SC60 comes in 20-pin DIPs and SOICs; SC64 comes in similar 24-pin packages. In lots of 100, the SC60 and SC64 cost $2.36 and $5.71 each, respectively. FG

Electronic Technology Corp., 2501 North Loop Dr., Ames, Iowa 50010; Scott Yeager; (515) 296-7000.
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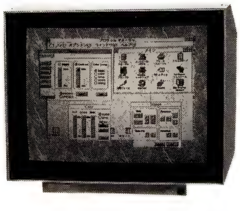
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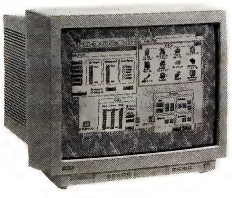
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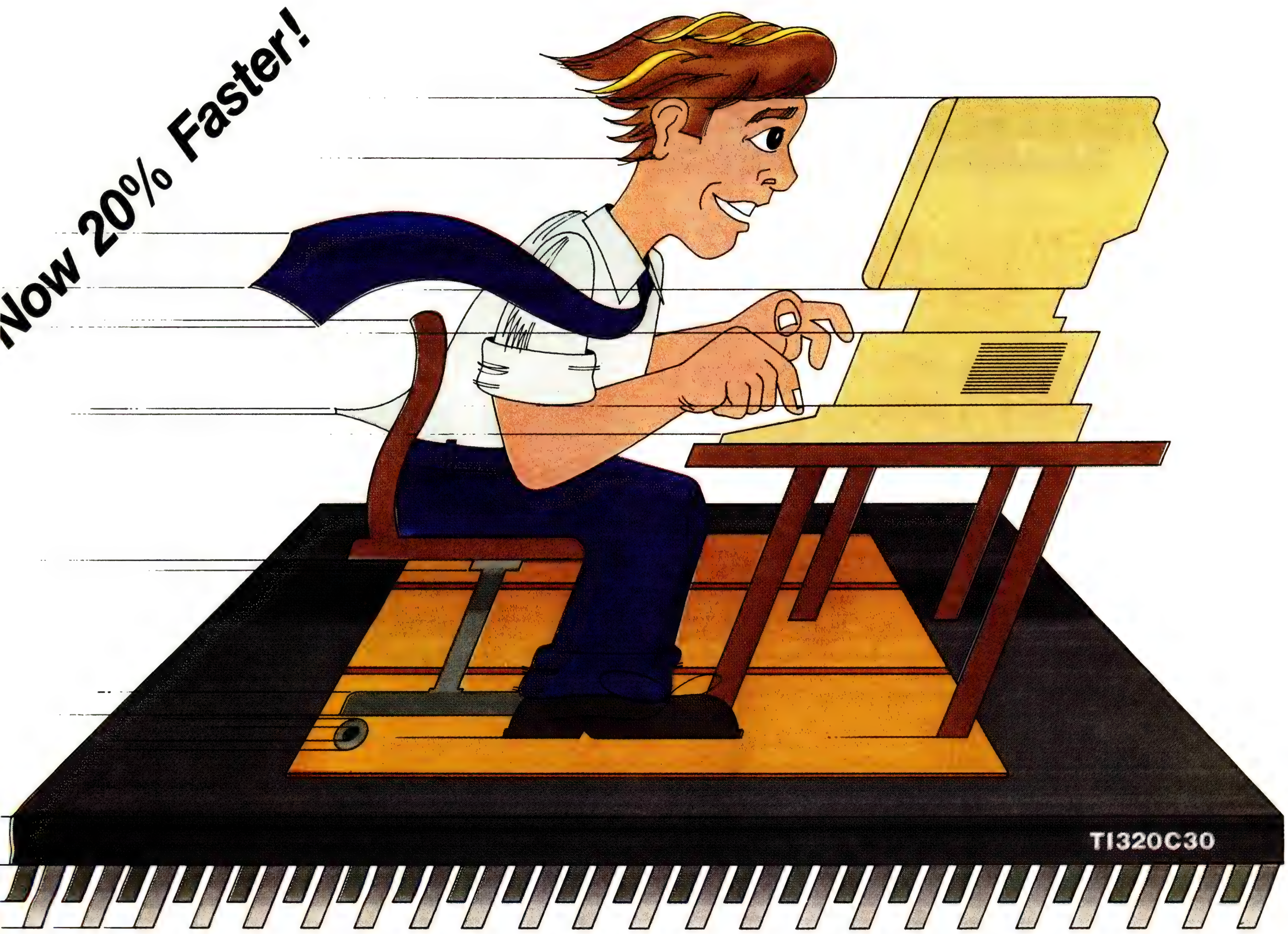


Beefed-up Banshee® II Blows Away Tough DSP Development Tasks

Banshee, ASPI's popular system board based on the Texas Instruments 'C30 Digital Signal Processor, now has a big brother. The new Banshee II boasts 4 Mbytes of zero wait-state static RAM and a speed increase to 40 MFLOPS.

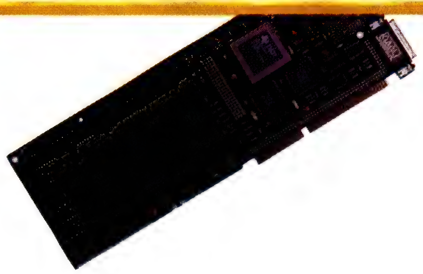
Banshee II is available with Ashell, ASPI's powerful development environment that turns your ordinary AT into an exceptionally powerful DSP workstation. With Ashell, you spend your time working on the DSP problem instead of coping with the computing environment.

Like its predecessor, Banshee II anchors a large family of interface boards and other devices; all are designed to take full advantage of the Banshee II's flexible I/O and memory architecture. Data acquisition options include A-D/D-A, digital audio, and serial audio and serial voice interfaces.

Users who need to develop special interface boards will find this task simplified by host bus, 'C30 memory bus, and 'C30 I/O bus connectors on the Banshee II board. For detailed specifications and prices, contact

Atlanta Signal Processors, Inc.,
1375 Peachtree St. NE, Ste. 690
Atlanta, GA 30309-3115
404/892-7265/Fax 404/892-2512

Banshee II



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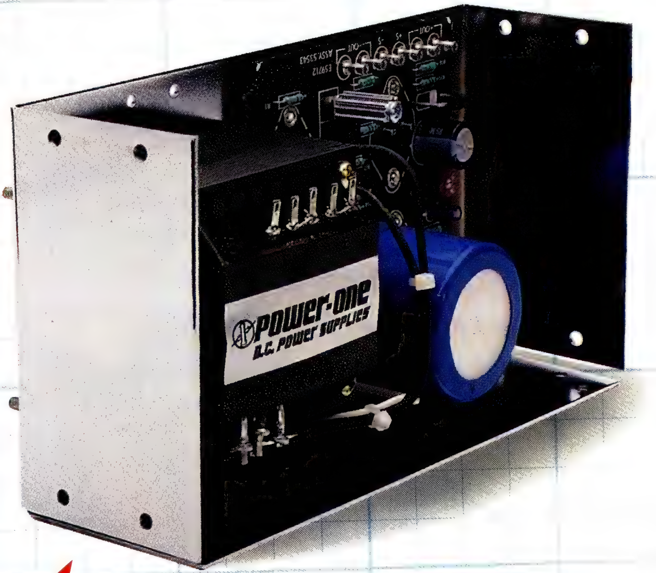

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VHDL-BASED PLD DESIGN TOOLS RUN UNDER WINDOWS NT

Engineers can create programmable logic devices (PLDs) with VHDL using the newest version of Altera's Max+Plus II design software. Version 4.0 adds VHDL synthesis to the PLD development environment that unifies design, compilation, and verification of Altera devices. In addition, version 4.0 shifts the system to a 32-bit environment operating under Windows NT.

A VHDL module in Max+Plus II version 4.0 employs architecture-specific synthesis algorithms that work directly from VHDL constructs to achieve maximum silicon efficiency. For example, addition operations described in VHDL are synthesized into Altera's SRAM-based Flex family using its carry-look-ahead feature, while the implementation into Altera's EEPROM-based Max 7000 family will utilize its logic-expander capability.

The VHDL module is coupled with the system's existing text-editor and error-location modules, which check for syntactical correctness and automatically highlight any errors in the VHDL source code. With the mixed-mode entry capability, engineers can describe their design using VHDL combined with schematics, Altera's hardware description language, and waveform descriptions. After compilation, Max+Plus II offers a variety of output options, including VHDL, Verilog, and EDIF net lists.

Advanced VHDL users will be able to use their knowledge of the language, along with any existing library of synthesizable VHDL designs, for Altera's high-density programmable logic devices. For PLD users who wish to learn VHDL, each copy of the software comes with the IEEE 1076 Reference Manual, the textbook *VHDL* by Douglas Perry, an Altera VHDL User Guide, and extensive on-line help.

For increased capacity and speed, Altera created Max+Plus II 4.0 using Microsoft's WIN32s software-development kit. Consequently, the full-32-bit implementation can run under Windows 3.1 or Windows NT. However, the company focused their development efforts on Windows NT, so Max+Plus II runs 20% faster on that platform.

Max+Plus II 4.0 runs on both PC and Unix platforms. The software is available now, and will be a free upgrade to all existing Max+Plus customers. The PLSM-VHDL module that provides VHDL-synthesis support is not included in the upgrade, but may be purchased for $3995. Unix versions of the VHDL synthesis are available for $6995.

***Altera Corp.**, 2610 Orchard Pkwy., San Jose, CA 95134-2020; (408) 894-7000.* **CIRCLE 717**

■ *LISA MALINIAK*

TRANSMISSION LIBRARY INCLUDES FIBER OPTICS

The Hypersignal for Windows Advanced Transmission Library from Hyperception provides a comprehensive set of design and analysis blocks for radio, wireline, and fiber-optic transmission systems. John C. Bellamy, author of *Digital Telephony*, designed these specialized blocks for use with Hyperception's block-diagram software simulator. The library includes block models for baseband transmission, modulation, demodulation, carrier and clock recovery, arbitrary filter design, system-performance measures, and other miscellaneous functions. Performance is measured with bit-error-rate simulations and calculations, eye patterns, and jitter analysis. Fiber-optic design is addressed with blocks modeling fiber-optic light sources, fiber transmission paths, automatic peak control, elastic storage, and universal asynchronous receiver/transmitters. In addition, there are examples demonstrating usage of each block. The Advanced Transmission Library is shipping now for $1495. LM

Hyperception Inc., 9550 Skillman, LB 125, Dallas, TX 75243; (214) 343-8525. **CIRCLE 718**

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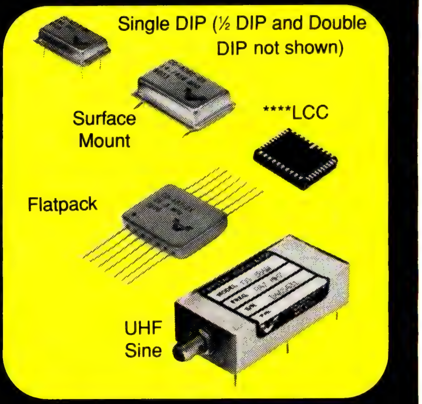

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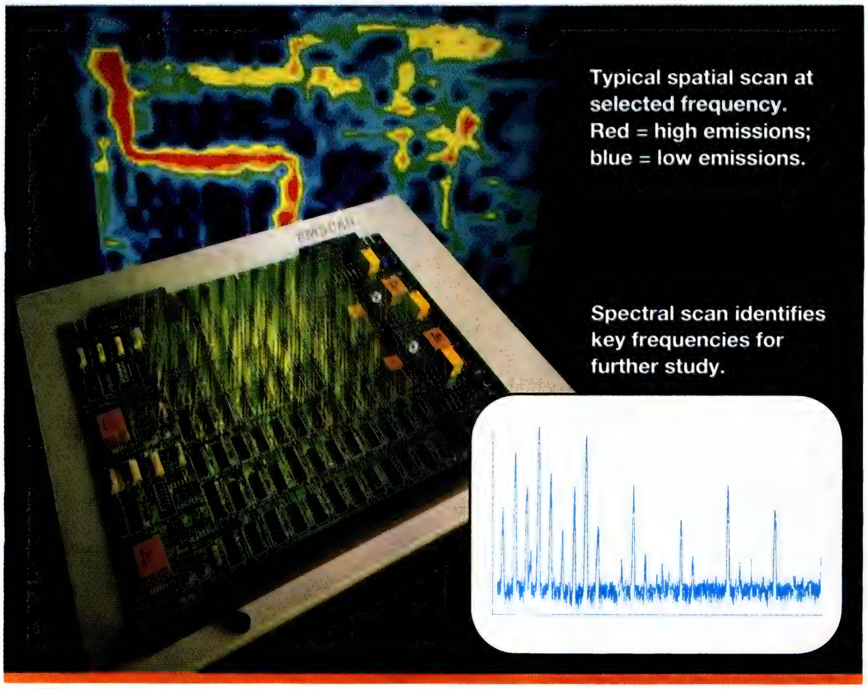

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Catch emissions problems at board level, where compliance fixes are least costly.

Now you can quickly get a color image of the electromagnetic performance of your printed-circuit board or subassembly *before* final compliance testing. Spatial and spectral displays generated by the EMSCAN PCB emissions scanner show you which frequencies and which areas of the board under test are guilty. These scans are stored for later comparison after design alterations, to check whether offending emissions are now down to acceptable levels.

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The software operates under "Windows" to make early diagnosis easy, even for those who are new to compliance testing. It can run on several PCs and workstations, and is readily ported to other environments for analysis.

You should learn all about this qualitative and quantitative measure of emissions for use during product development—where design corrections are least costly. To start, call toll-free (1-800-933-8181) to speak with an applications engineer and arrange to see a demonstration in your office or plant.

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HIGH-SPEED VHDL TOOL HAS GRAPHICAL FRONT

The Optium VHDL simulator from Vantage is based on the company's new high-speed simulation engine called SpeedWave, and sports a graphical interface based on Motif. The interface creates an intuitive user environment, including a browser and watch window that aids in traversing the design hierarchy and monitoring comparative signal values. Also, Vantage has optimized the strengths of Motif by reducing the number of commands needed to implement frequently-used features like locating and editing signal values and entities. The core of Optium is the SpeedWave simulation engine. Vantage claims that SpeedWave provides up to two times faster performance than other VHDL simulators. Part of the reason is a new approach to streamlining signal representation, called Bi-Level Adaptive Signal Trees (Blast). Blast reduces the time needed to process information, and creates an efficient architecture. Optium runs on Unix workstations. It's shipping now for $16,000. LM

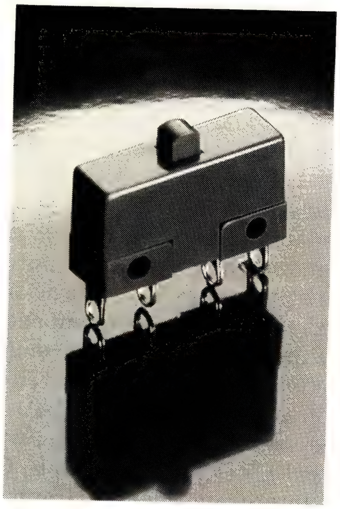
Vantage Analysis Systems Inc., 47211 Lakeview Blvd., Fremont, CA 94538; (510) 659-0901.

CIRCLE 719

TOOL AIDS NONLINEAR CONTROLLER DESIGN

The Nonlinear Control Design (NCD) Toolbox from The MathWorks helps engineers create automatic controllers for nonlinear systems in industries such as automotive, aerospace, process control, and petrochemicals. With NCD, control engineers can work directly in the nonlinear domain, bypassing previously used methods like linear approximation. The NCD Toolbox is part of the company's Matlab technical computing environment. It also works with The MathWorks' Simulink block-diagram environment for modeling and analyzing dynamic systems. NCD Toolbox runs on PCs under Windows, and on Macintosh and Unix-based computers. Pricing for the Windows version starts at $895. LM

The MathWorks Inc., 24 Prime Park Way, Natick, MA 01760; (508) 653-1415. **CIRCLE 720**



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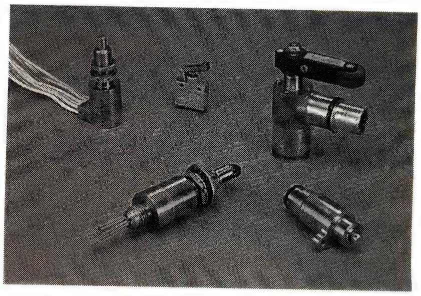

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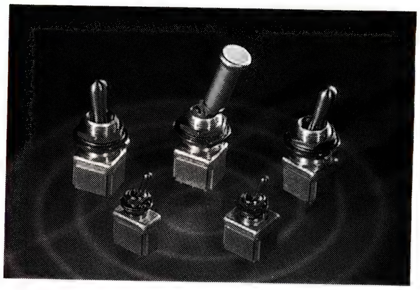

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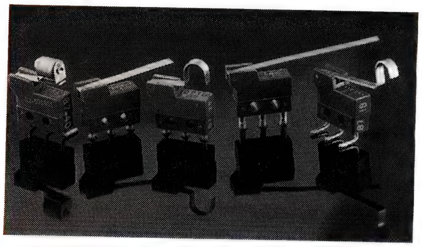

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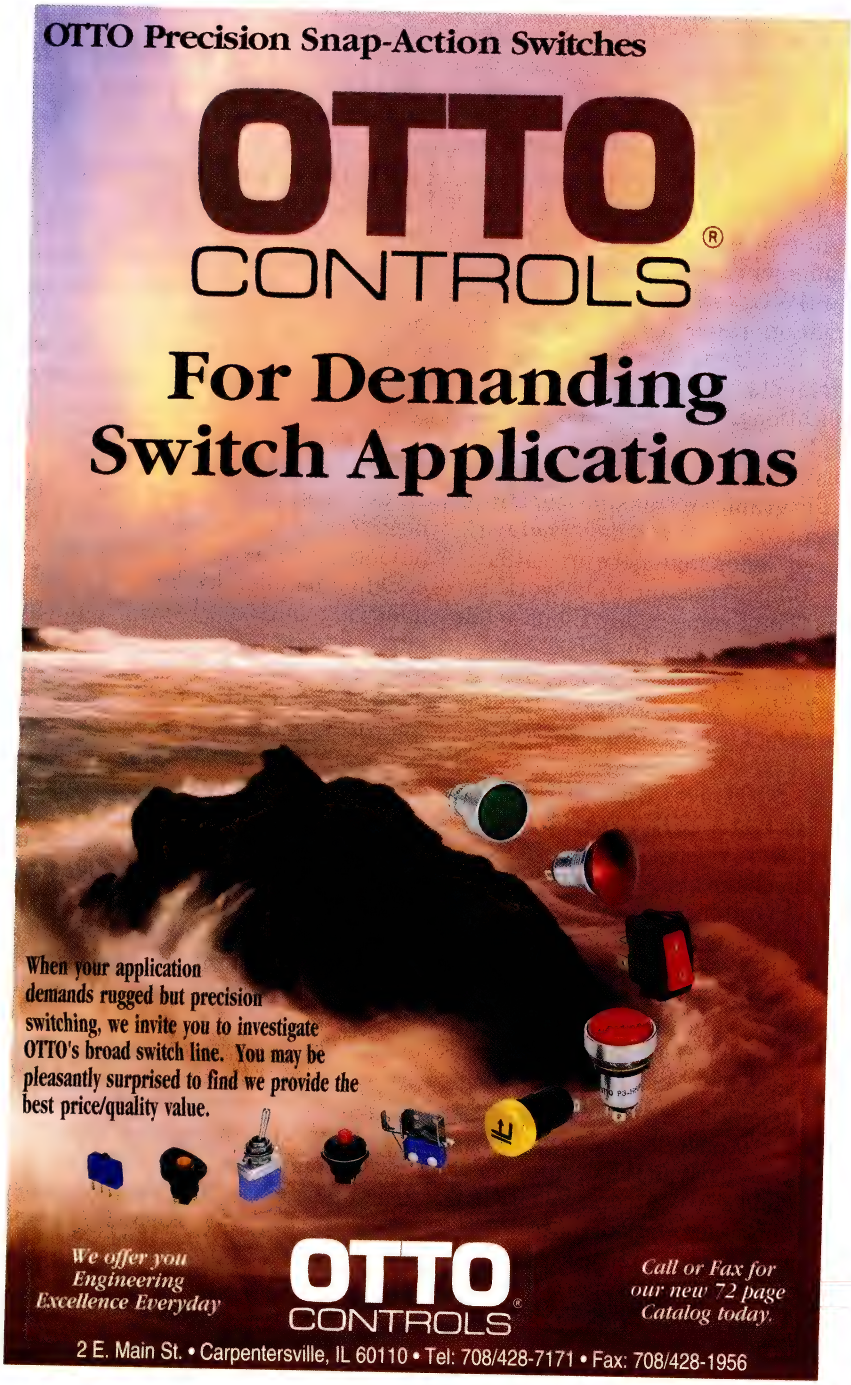

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READER SERVICE 149

MODEL LIBRARY AIDS COMMUNICATIONS DESIGN

A new module added to Comdisco's Bones family of network-performance analysis tools helps engineers plan communication systems using frame relay, a fast-packet technology for enterprise-wide networks. With the Bones software, users specify network topologies, interconnect devices, and traffic flow by joining graphical icons that represent the network components. Traffic is characterized using a variety of techniques, including recorded traces of actual network traffic, scripts describing typical network traffic, and statistical traffic generators. The new Frame Relay Cloud module lets users model high-speed multiplexed data transfer in both public and private networks. Engineers use a parameter-based library to determine the number of permanent virtual circuits (PVCs) and the committed information rates (CIRs) needed to meet the transaction-response requirements of their mission-critical applications. They can specify access rate, CIR, committed burst size, and transit delays. The library includes built-in graphs of transmission, transit, and total frame delays; network offered load; and network utilization. Bones runs on Unix workstations. The Frame Relay Cloud module is shipping now for $4000. LM

Comdisco Systems Inc., 919 E. Hillsdale Blvd., Foster City, CA 94404; (415) 574-5800. **CIRCLE 721**

CAD TOOL INTERFACES WITH EDA SOFTWARE

The newest release of the Pro/Engineer mechanical CAD software adds Mentor Graphics' products to the list of electrical CAD tools to which it interfaces. Pro/Engineer creates 3D components from 2D electrical-CAD outlines by extruding the profile to a given height or by mapping to a Pro/Engineer library component. This permits engineers to evaluate critical interference, best fit, and mass properties early in the design, which may avoid costly errors. Pro/ECAD is an interface option that directly exchanges information between Pro/Engineer and supported electrical CAD systems. That support permits products with both mechanical and electrical components to be developed concurrently. Changes that are made in the mechanical design can update the electrical design, and vice-versa, at any point in the product-development cycle. Information such as board outline, component profile and location, and placement restrictions may be transferred in both directions. The Pro/ECAD interface combines Pro/Engineer with electrical CAD packages from Cadence, Intergraph, Mentor Graphics, and Racal-Redac. Call the company for pricing and additional product information. LM

Parametric Technology Corp., 128 Technology Dr., Waltham, MA 02154; (617) 894-7111. **CIRCLE 722**

IMPROVED LAYOUT TOOL UPS DENSITY BY 25%

Version 4.0 of the L-Edit/SPR ASIC place-and-route software includes new optimization routines that offer an order of magnitude improvement in layout time, and up to 25% higher layout density than did previous versions. L-Edit/SPR 4.0 provides placement and routing for ASIC standard-cell design, automatic padframe generation, and padframe routing. The new version can operate on circuits having twice as many elements as could be handled by Version 3.0. In addition to improved speed and density, a number of features afford users more control. For instance, a Time Factor Control determines the length of time used by the placement optimizer. For most applications, a pre-assigned default setting provides the optimum starting condition. Users can specify other run times by modifying one input parameter. Chip size is reduced with a new Row Evener parameter that minimizes the length of the longest cell row, and keeps cell rows even. Global routing optimization is another new feature that seeks an optimal path for each net to minimize net size and to maximize wiring density. The L-Edit/SPR 4.0 software supports personal-computer, Macintosh, and Unix platforms. Pricing for those platforms starts at $995, $1495, and $2995, respectively. LM

Tanner Research Inc., 180 N. Vinedo Ave., Pasadena, CA 91107; (818) 792-3000. **CIRCLE 723**

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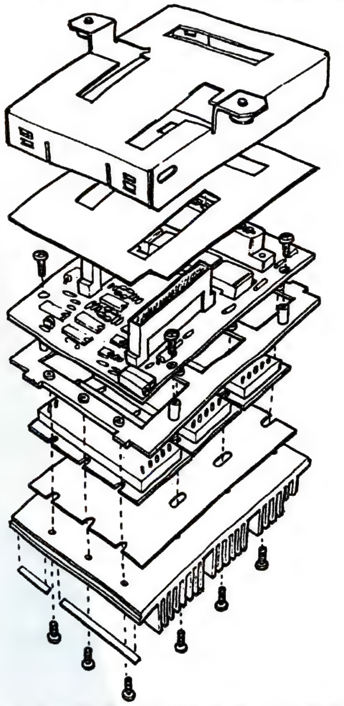

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FIB 200 Focused Ion Beam Workstation

A free brochure on the FIB 200 Focused Ion Beam (FIB) Workstation from FEI Company, Beaverton, Ore., details the workstation's features and specifications. The FIB 200 provides fast, accurate milling and deposition of submicron structures. Although designed for smaller samples, such as wafer sections and packaged semiconductor parts, the lower-cost FIB workstation offers the same techniques and applications capabilities as 8-in. wafer-compatible FIBs. Applications included are a cross-section preparation of scanning-electron microscopy and transmission-electron-microscopy specimens, high-contrast imaging, gain structure analysis, and fabrication of micro-electromechanical structures. CM **CIRCLE 797**

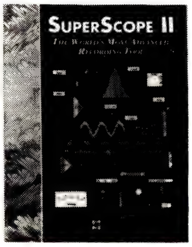
TUTORIAL DESCRIBES SONET/SDH TESTS

A comprehensive 10-page tutorial from Microwave Logic, Chelmsford, Mass., discusses jitter and wander testing on Sonet/SDH systems. The publication talks about the differences between jitter and wander; the causes of line jitter; and the ANSI, Bellcore, and CCITT limits specified for jitter generation, jitter transfer, jitter tolerance, and interference jitter. A typical test setup for measuring each of these parameters is shown. A separate section on wander discusses time interval error, maximum time interval error, and time deviation. The tutorial suggests ways to test for each. JN **CIRCLE 792**

LEAD-FREE SOLDER REPLACEMENTS

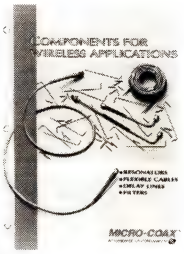
A new report from BPA Technology and Management, Cold Spring Harbor, N.Y., titled "Conductive Adhesives And Solder Replacement," reviews the status of lead-free solder and conductive adhesive programs. In addition, the report analyzes current applications, and forecasts both usage and market size. According to BPA, 1.5 million tons of consumer electronic products are disposed of in land fill sites in Germany every year. All of these products contain lead that can leach into the earth and contaminate drinking water supplies. BPA notes that a lead-free environment and the increased investment needed for fine-pitch assembly has accelerated industry programs directed to the development of materials and processes for a lead-free component joint. CM **CIRCLE 793**

SUPERSCOPE II BROCHURE


SuperScope II

A 16-page, full-color brochure from GW Instruments, Somerville, Mass., describes SuperScope II, a Macintosh-based software package that can digitize, analyze, calculate, graph, and database waveforms in real-time, with the help of data-acquisition hardware available from GW Instruments. SuperScope II includes standard ready-to-go instruments, such as a strip-chart recorder, oscilloscope, spectrum analyzer, and YX recorder. The software can digitize long continuous waveforms, spool them to disk, plot and analyze every point, allow on-line annotation, and then allow post-acquisition viewing. The brochure is available free of charge. CM **CIRCLE 794**

COMPONENTS FOR WIRELESS APPLICATIONS


COMPONENTS FOR WIRELESS APPLICATIONS

MICRO-COAX

Micro-Coax, Collegeville, Pa., has a brochure that covers its complete line of components for wireless applications. The brochure features miniature coaxial components, UTiFLEX miniature flexible cables, custom delay lines, and In-A-Cable filters. The miniature coaxial components are low-profile designs used as resonators in DRO and VCO tank circuits; as impedance inverters; and as transmission-line filters, time-delay elements, and shielded interconnects. UTiFLEX miniature coaxial cables are good for on-board interconnects, rack module interconnects, and antenna-to-receiver links. Micro-Coax custom delay lines are available with short or long intervals and as active types that provide the lowest loss. The brochure, *Micro-Coax Components for Wireless Applications*, provides complete specifications and applications information about the company's products, and it's available for free. CM **CIRCLE 795**

VIDEO OFFERS HELP FOR HARMONIC PROBLEMS

"Managing Harmonics" is a video tape (VHS) that explains the causes of harmonic voltages and currents in power-distribution systems. The tape also offers ways to deal with the problem. Available for $19.95 from Fluke Corp., Everett, Wash., the videocassette is designed for anyone who has a working knowledge of harmonics but still needs help with existing harmonic problems. Described in the video are symptoms—such as overloaded neutral wires, hot transformers, and tripping circuit breakers—and ways to both identify and manage the harmonics that cause them. The tape also introduces the Fluke Model 40 Power Harmonics Meter and Model 41 Power Harmonics Analyzer. A more basic video, "Understanding Harmonics," is also available. JN **CIRCLE 796**

T&M CATALOG INCLUDES FULL RANGE OF PRODUCTS

The 1994 Tektronix Test and Measurement Catalog features comprehensive product specifications for users of test equipment in digital design, general purpose, telecommunications, television, industrial, and semiconductor applications. Also included is information on computer graphics products and customer support. For the first time, Tek's catalog contains products from Advantest in the rf, microwave, and telecommunications area and from Rhode & Schwarz. Last year Tektronix, Wilsonville, Ore., became the exclusive distributor for Advantest in North America and for Rhode & Schwarz in the U.S. A four-color New Products section highlights recently introduced instruments, accessories, and enhancements. The catalog is free. JN **CIRCLE 798**

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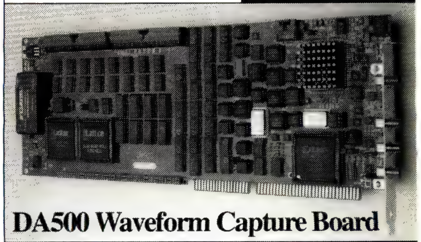

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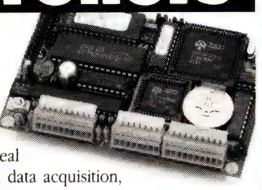

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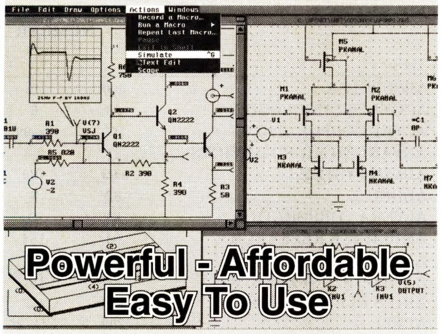

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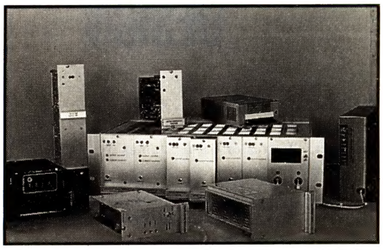

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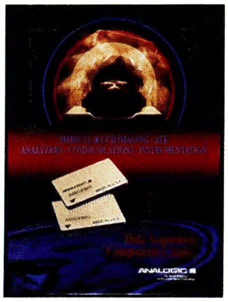

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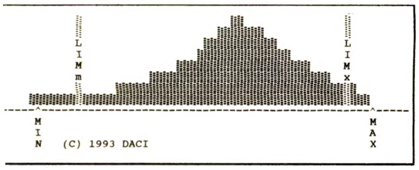

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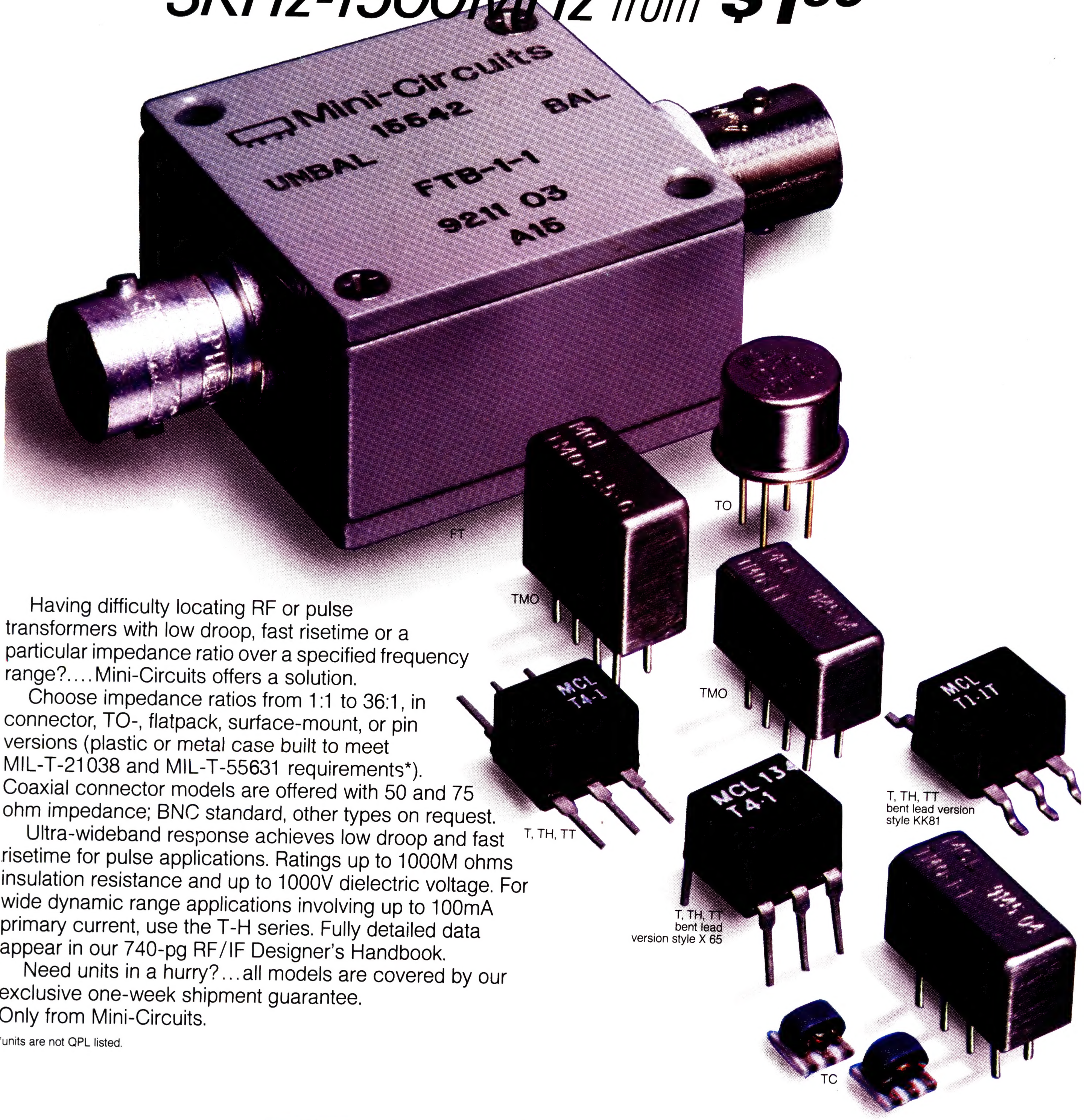

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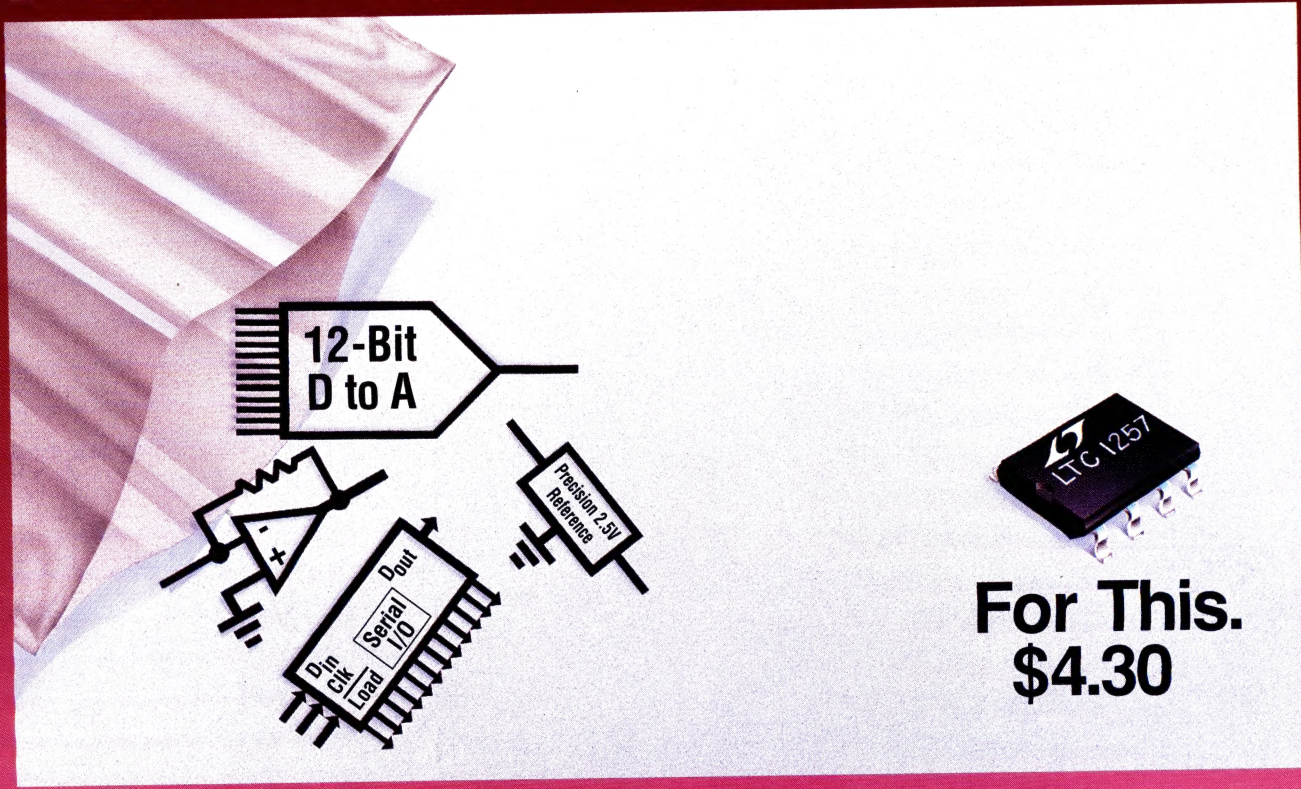

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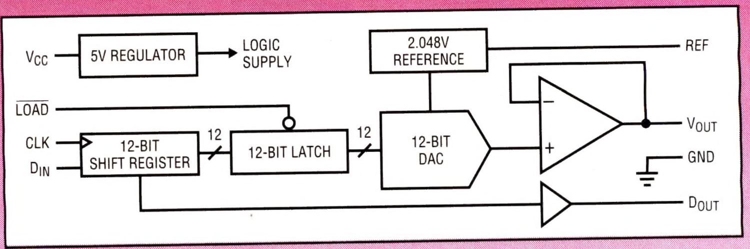

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